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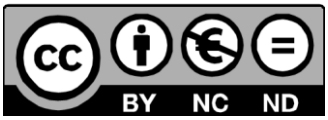

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Introduction

In recent years, the development of advanced communication standards and modern digital telecommunication systems demands a continuous improvement of the RF performances in terms of output power, bandwidth, efficiency and signal fidelity. The most crucial part of any communication system is the active transistor which is capable of predicting the performances of the complete system. Therefore, the focus on the microwave transistors have been significantly increased over the last few years, and much of the research activities have been specifically devoted to the development of suitable device technology that would meet the ever-increasing demands of the future electronic innovations. For instance, higher efficiency, higher speed, low power and wider band-width are intensely required for wireless portable communication systems whereas satellite based systems and TV broadcasting require device technology which is capable of operating at higher frequencies and higher output power, in order to reduce the overall size of the complete system.

The semiconductor industry has been dominated by silicon technology for more than a decade and the major factor contributing to the growth of the industry is the scaling of devices. Currently, 11/10-nm node technology is considered to use in industrial applications and 7-nm node is expected to appear in RF market by the year 2018, and 5-nm node by 2020. Moreover, the easy availability of Si by nature is another reason for its huge success in semiconductor industry. The scaling of device leads to the improvement in device RF performances, however the Si based devices are rapidly approaching their maximum theoretical limit of operation and therefore, they are not capable of delivering the performance demanded by the future RF and microwave applications. Furthermore, the low carrier mobility and saturation velocity impedes its suitability for modern electronic applications such as TV broadcasting and mobile communications. Hence, a research on new materials such as SiGe, SiC and group III – V semiconductors have been investigated to replace the existing silicon technology. The conventional group III – V materials has already demonstrated its remarkable success in optical applications. However, the narrow bandgap property of these materials limits their ability for high power and high temperature applications. Moreover, group III – Nitrides promises improved performance advantages over conventional group III – V semiconductors because of their direct and wide bandgap. Among group III– Nitrides, GaN material has been considered as the promising material for both optical and microwave high power applications. Although GaN-based optical devices have been widely used in commercial applications, GaN-based

microwave device technology is relatively immature until today that restrains the widespread commercialization of these devices. However, GaN-based devices have demonstrated remarkable performances to meet the ever-increasing demands of the communication market. The superior electron transport properties of GaN material makes this GaN technology feasible for applications ranging from commercial to military.

The AlGaN/GaN High Electron Mobility Transistors (HEMTs) have been emerged as the promising candidates for high-power microwave and mm-wave applications. The superior physical properties of GaN material along with its potential to create hetero-structure device makes this device capable of operating at higher frequencies. Moreover, the presence of spontaneous and piezoelectric polarization charges increases the two-dimensional electron gas (2DEG) density in the channel, without the requirement of any intentional doping in the device. The large bandgap offset formed between the AlGaN and GaN materials forms a quantum potential well like structure to accommodate the 2DEG closer to the hetero-junction interface. Therefore, the electrons present in the quantum well possess extreme high mobility, due to the absence of doping which causes the increased ionized impurity scattering effects. The 2DEG sheet carrier density (n_s) achieved in GaN HEMTs is well above $10^{12} – 10^{13}$ cm^{-2} which is very much higher compared to other group III – V semiconductors. Furthermore, the improvement in the DC and RF performances of GaN HEMT devices, over the years, has been widely reported in the literature.

Over the years, there has been remarkable progress dedicated to the growth of GaN HEMT device technology including improving the quality of hetero-structure epitaxial layers, passivation layers and materials used for passivation, selecting the best substrate materials, optimizing the barrier thickness, implementing gate-recess techniques and adoption of field-plates, either gate or source connected. All these technological improvements further extend the boundaries of GaN HEMT device performance. However, the presence of traps in the structure significantly degrades the device performance and also detriments the device reliability. The origin of these traps and their physical location in the device remains unclear. Trapping effects in the device causes current collapse, output admittance dispersion, transconductance dispersion, gate-lag, and drain-lag and also contribute to low frequency noise. Moreover, the presence of traps also causes increased gate-leakage, hot-electrons based device degradation and stress-induced defect generation.

In this thesis, a part of the research activities has been specifically devoted to understand the trapping mechanisms and its physical locations in the device structure using experimental characterization and physics-based TCAD Sentaurus device simulations. The experimental techniques such as Low-Frequency S-parameters measurement, Low-Frequency Noise (LFN) measurement and drain-lag characterization have been used for characterizing the traps existing in GaN/AlGaN/GaN HEMT devices. Furthermore, we have used TCAD physical simulations to identify the physical location of traps in the device.

The second part of the thesis is focused on characterizing the AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrates. As the demand for high frequency performance of GaN-based HEMTs are increasing over time, it is often necessary to implement ultra-short gate lengths and using of thin AlGaN barrier. However, these processes significantly degrade the performance of AlGaN/GaN HEMT devices. Therefore, AlN/GaN HEMT devices are receiving much attention these days and also considered to be a suitable alternative to replace conventional AlGaN/GaN HEMT devices. The AlN/GaN HEMT devices is capable of delivering high drain current (~2A/mm), high breakdown voltage and lower on-resistance (R_{ON}), even using ultra-thin AlN barrier. The second part of the thesis is composed of three different research sections. (i) The first section focusses on investigating the impact of GaN channel traps on the performance of AlN/GaN/AlGaN HEMT devices using two-dimensional (2D) TCAD-based physical simulations. (ii) Obtaining a lower R_{ON} after an OFF-ON switching event is a critical requirement for power switching applications. Moreover, the temperature has also a significant influence on R_{ON}. Therefore, we attempt to extract the temperature-dependent R_{ON} of the AlN/GaN/AlGaN HEMT devices using on-wafer measurements and TCAD-based device simulations. Furthermore, we propose a simplified technique to extract the temperature- and bias-dependent channel sheet resistance and parasitic series contact resistances of this device technology. (iii) In the third section, we have made a comprehensive evaluation of thermal behavior of AlN/GaN/AlGaN HEMTs grown on Si and SiC substrates through three-dimensional (3D) TCAD thermal simulations and on-wafer measurements. Using pulsed *I-V* measurements, the thermal resistance (R_{TH}) for various device geometries have been extracted. Furthermore, TCAD thermal simulations have been performed for the similar device geometries and the R_{TH} have been extracted and verified with measurement results.

The organization of the thesis is described as follows:

Chapter 1 introduces the physical properties of GaN material, importance of GaN HEMT technology compared to other existing device technologies. The key challenges and reliability issues of GaN-based devices such as current-collapse, gate-lag, drain-lag, self-heating and hot-electrons degradation effects and gate-leakage have been described in detail.

Chapter 2 describes the physics based analytical modeling of current-voltage characteristics of AlGaN/GaN HEMT devices. A generalized drain current model, valid for predicting both intrinsic and extrinsic characteristics have been presented. Chapter 2 also provides an overview of the TCAD Sentaurus simulation tool used in this thesis. The basic semiconductor equations and different kind of physical models existing in the simulation tool have been described. The illustration of formation of the two-dimensional electron gas (2DEG) in AlGaN/GaN HEMT device using TCAD physical simulations have been provided. The comparison of simulation results of different kind of simulation models have also been discussed.

Chapter 3 investigates the trapping mechanisms of GaN/AlGaN/GaN HEMTs grown on SiC substrate using Low-Frequency measurements and TCAD-based physical device simulations. The extraction of activation energy and cross section of the traps existing in the device using LF measurements have been explained. The TCAD physical simulation model calibration procedure has been discussed in detail. The identification of physical location of traps using TCAD physical simulations have been discussed.

Chapter 4 explores the influence of GaN channel traps on the performance of AlN/GaN/AlGaN HEMTs grown on SiC substrate using TCAD-based physical device simulations. The impact of both donor-like and acceptor-like traps on the device performance have been studied. In the second part of this chapter, the temperature dependent study of on-resistance of this device technology have been analyzed using on-wafer measurements and TCAD simulations. Moreover, a simple methodology to extract the temperature and bias-dependent parasitic channel sheet resistance and contact resistance of the device have been proposed.

Chapter 5 investigates the thermal resistance extraction of AlN/GaN/AlGaN HEMTs grown on different substrates using on-wafer pulsed I-V measurements and 3D-TCAD thermal simulations. The thermal resistances extracted using measurements and TCAD simulations have been discussed in detail. Then, the simulated transient thermal behavior of the device and its respective modeling using modified recursive network have been described.

Finally, the results obtained in previous chapters have been summarized and the necessary conclusions are drawn. It also outlines the scopes of the future work based on the results obtained in this thesis.

Chapter 1

Introduction to basics of GaN HEMT Technology

Chapter 1. Introduction to basics of GaN HEMT Technology

1.1. General Introduction

Modern wireless communication systems such as portable mobile devices and base stations require an RF power amplifier with high linearity and efficiency. The most crucial component of any RFPA is the active device, which is capable of determining the performances of RFPA in terms of gain, output power, efficiency, bandwidth and linearity. The dominant technology currently in use for the design of high power RFPAs is the Si LDMOSFET. However, the development of modern communication systems demands the active device to operate at higher frequencies with higher output power. The established Si based LDMOS device technology in the current RF market is capable of covering only a frequency range from few hundred Mega hertz (MHz) up to a maximum of 3.8 Giga hertz (GHz) [1.1], [1.2]. Hence a good deal of research on new semiconductors such as SiC, GaAS and GaN and other wide band gap materials has been undertaken in recent years to replace the conventional Si technology at high frequencies. The GaAS MESFET devices are capable of operating at high frequencies due to their bulk high electron mobility value, but the thermal conductivity is approximately only one third, when compared to Silicon that makes this technology feasible only for low power applications [1.3]. SiC MESFETs are also suited for high temperature and high voltage operations due to its material properties. However, the SiC devices lack the potential of forming a hetero-junction and hence have low electron mobility which impedes their capability for high frequency applications. Among others, Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) device technology has proven to be the best and most successful device for microwave high power and RF applications so far. The superior material properties of GaN together with the hetero-structure device make GaN technology capable of operating from a few hundreds of MHz to 100 GHz [1.4].

1.2. Brief History of GaN HEMTs

GaN HEMTs are still considered to be relatively immature technology when compared to conventional GaAs HEMTs and Si LDMOSFET technologies. However, most of the recent research work has been primarily focused on the improvement of GaN HEMT technology, in order to become a disruptive technology for RF and microwave power applications. Khan *et* al. [1.5] reported the first AlGaN/GaN hetero-junction transistor in 1992, the two-dimensional electron density (2DEG density) in the channel was observed in the order of 10^{11} cm^{-2} and the electron mobility was in the range of 400- 800 $cm^2/V.s$. Moreover, they were the first group to

report the DC and RF performance of GaN HEMTs in the consecutive years, 1993 and 1994, respectively [1.6], [1.7]. The saturation drain current of 40 mA/mm was reported for 0.25-µm gate length device [1.7]. In 1996, Wu *et* al. [1.8] reported a RF power density of 1.1 W/mm at 2 GHz for AlGaN/GaN HEMT. Over the years, the improvement in the performances of AlGaN/GaN HEMTs have been largely reported in the literature. The power density of 40 W/mm at the operating frequency of 4 GHz was reported in [1.6]. An extreme high output power of 500 W at L-band was reported in [1.9]. Moreover, in recent years, some remarkable combinations of high output power (P_{out}), high power-added efficiency (*PAE*), high break-down voltage, maximum cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) have been reported. Kimura *et* al. [1.10] reported 43% PAE with an output power of 60-W at X-band, and Yamasaki *et* al. [1.11] demonstrated 68% PAE with 100-W output power at C-band. A maximum current density of 750 mA/mm with a current gain cut-off frequency of 90 GHz has been reported [1.12] for a 0.1-µm gate length AlGaN/GaN HEMT grown on Si substrate. For a 0.9-µm AlGaN/GaN HEMT on Si substrate, f_T and f_{max} of 100 and 206 GHz, respectively have been reported in [1.13]. The break-down voltage (V_{BR}) of 1500 V has been reported for AlGaN HEMT on Si substrate in [1.14]. Similarly, the highest break-down voltage of 1700 V has been reported for AlGaN HEMT grown on Sapphire substrate in [1.15]. A PAE of 34.2%, P_{out} of 2.5 W/mm, f_T of 149 GHz and f_{max} of 285 GHz have been reported at 87 GHz in [1.16]. Moreover, the state-of-the-art of AlGaN/GaN HEMTs for LNA and RF power amplifier applications have been reported in [1.17]–[1.19]. Regardless of the reported performances, the commonly observed output densities are in the range of 12 W/mm and the drain current is in the range of ~1 A/mm, respectively. The performance of the AlGaN/GaN HEMT devices can be further improved by implementing the ultra-short gate lengths and using of thin AlGaN barrier. However, reducing the thickness of the AlGaN barrier below a certain extent (10-nm) causes the strongest degradation of 2DEG density in the channel [1.20]. Therefore, in recent years, AlN/GaN HEMT devices are gaining much attention because of their capability of achieving higher current density (2A/mm), using an ultra-thin AlN barrier [1.20]. The maximum drain current (I_{Dmax}) of 3 A/mm, with f_T and f_{max} of 454 and 444 GHz, respectively has been reported [1.21] for 20-nm gate length AlN/GaN HEMT device grown on SiC substrate. A PAE of > 33% and P_{out} of 2.3W/mm at 40 GHz have been reported [1.22] for 0.1-µm AlN/GaN HEMT devices grown on Si with an ultra-thin AlN barrier of 6-nm. The I_{Dmax} of 1.5 A/mm and with f_T of 370 GHz have been reported for 0.3-µm InAlN/AlN/GaN HEMT devices in [1.23]. In summary, the last decade has witnessed the substantial amount of research work has been devoted to GaN HEMTs and hence the performance has improved significantly.

1.3. Material Properties of GaN and other Related Technologies

The material properties of devices for RF high power applications are listed in Table 1.1 [1.19]. The GaN material has high band gap energy and high electric break down strength, which can translate into high transistor operating voltages and high breakdown voltages of GaN devices [1.18]. The high saturation velocity causes the high output power delivered from small sized GaN devices, which makes this GaN technology more compatible for high power applications.

Table 1.1. Typical comparison of physical properties of semiconductors for RF/microwave power applications [1.19].

Parameter	Si	GaAs	4H-SiC	GaN	Significance
Band gap (eV)	1.1	1.42	3.26	3.39	High operating voltages; High temperature operation
Electron Mobility ($cm^2/V.s$)	1350	8500	700	1200	High DC gain; High operating frequency
Dielectric Constant	11.8	13.1	10	9.0	Lower capacitance and it reduces the parasitic delay.
Breakdown Electric field (M.V/cm)	0.3	0.4	3.0	3.3	Higher operating voltage; High output impedance; Ease of impedance matching
Electron saturation velocity, V_{sat} (10^7 cm/s)	1.0	1.0	2.0	2.5	High output current density; High DC gain
Thermal conductivity (W/cm.K)	1.5	0.43	3.3-4.5	1.3	Smaller die size; Efficient heat dissipation
Lattice constant (Å)	5.4	5.7	3.1	3.2	Smaller the difference in the lattice constant between GaN and SiC (substrate) reduces the density of defect.
JM	1	2.7	20	27.5	Determines the power-frequency limits of the material

The small size devices further implies that these devices have higher input and output impedances and it eases the low loss impedance matching [18]. The GaAs material has a high electron mobility and large electron saturation velocity, however the break-down electric field is limited to 0.4 MV/cm and hence, it is suitable only for medium power applications. Moreover, GaN-based HEMTs can achieve higher electron mobility than GaN MESFETs due to the isolation of dopants far away from the 2DEG channel, attributed to reduced impurity scattering effects. Johnson's figure of merit (JM) represents the power-frequency limit of the material. A JM value of < 3 implies that the material is suitable only for low power applications. It is evident from Table 1.1, GaN material has the highest JM which makes them ideal for high power and high frequency applications. The high carrier concentration and high electron mobility lead to a lower on-resistance (R_{ON}) which is crucial for power switching applications. All these unique material properties of GaN devices are the primary reason for their better performance compared to the Silicon RF MOSFETS. However, the GaN technology is relatively immature and is quite expensive. The commercially available GaN HEMT devices either use Silicon (or) Silicon Carbide (SiC) as a substrate material. The GaN-on-SiC HEMT demonstrates superior performance than GaN-on-Si HEMT due to the high thermal performance of the SiC substrate which allows efficient heat dissipation. This is particularly important for high power and high frequency applications. However, in recent years, the state-of-the-art has also been reported for the AlGaN/GaN HEMT devices grown on Si substrate [1.13].

1.4. AlGaN/GaN High Electron Mobility Transistor (HEMT)

A High Electron Mobility Transistor is an heterostructure device composed of two different layers in which the wide band gap material is grown over the narrow band gap material. The energy band diagram of the HEMT device before forming the hetero-junction is shown in Fig. 1.1 (a). When the wide band gap material is brought into contact with the narrow band gap material, the hetero-junction interface is formed with the necessary band bending to form a 2DEG (Fig. 1.1 (b)). The electrons of donor impurities in the wide band gap material (AlGaN), diffuse across the hetero-junction interface to the narrow band gap material and there they are confined due to the potential barrier formed by the hetero-junction interface. The electron transfers take place owing to the differences in the electron affinities (Ψ_s), band gap (E_g) and work function ($q\varphi_s$) of these two materials. This electron transfer process continues until a Fermi level is balanced between two materials and the equilibrium condition is achieved. The

quantum potential well formed at the hetero-junction interface is shown in Fig. 1.1 (c) and is narrow enough to accommodate the free electrons.

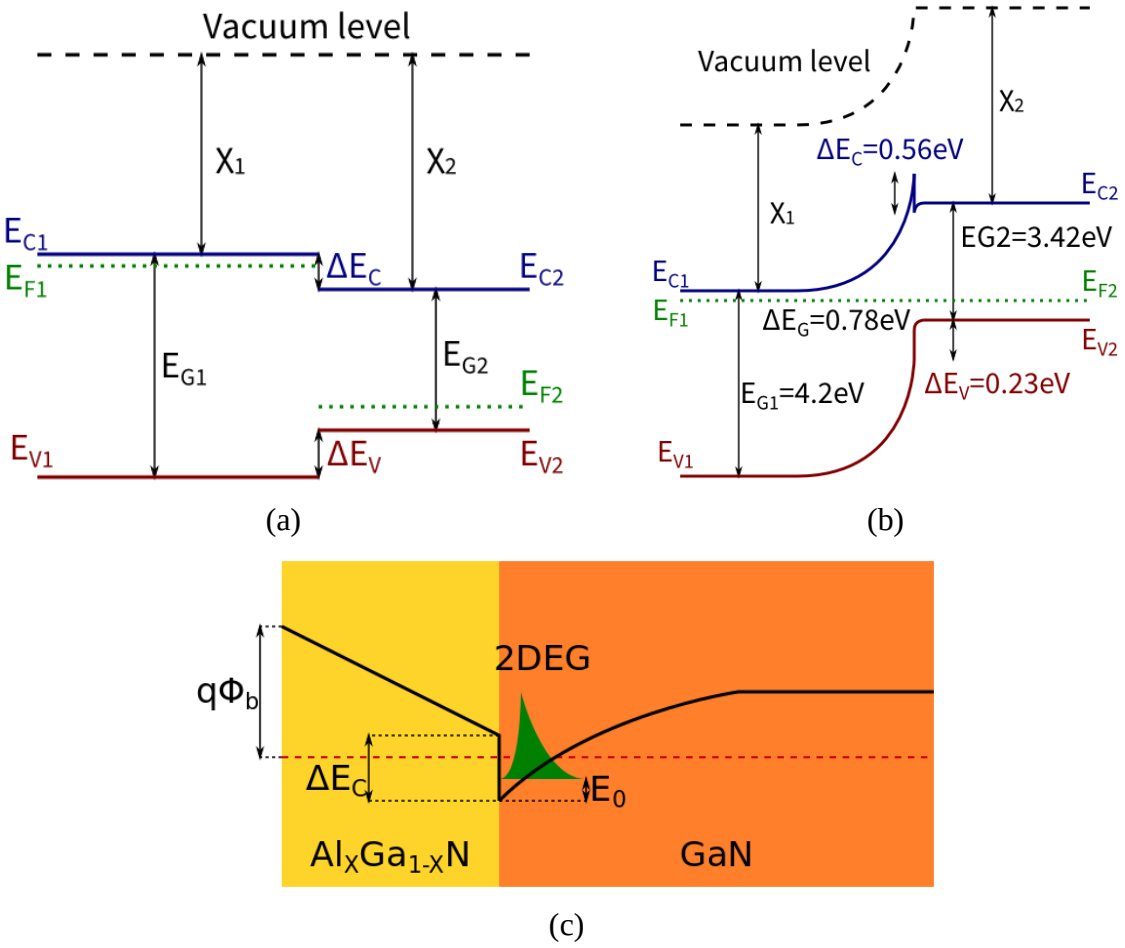


Fig. 1.1. (a) Energy band diagram of AlGaN/GaN HEMT illustrating band gap discontinuity (a) before forming the hetero-junction (b) band bending due to hetero-junction formation (c) 2DEG at the hetero-junction interface.

The electrons confined in the quantum well are separated from the ionized donor atoms and thereby possess extremely high mobility and are generally considered to be two-dimensional electron gas (2DEG), which is the unique property of HEMT. The formation of 2DEG in AlGaN/GaN HEMT at the hetero-junction is different from that of the conventional AlGaAs/GaAs semiconductor. GaN is a polar crystal and it exhibits strong polarization effects at the AlGaN/GaN hetero-junction interface. The strong polarization effects induce high electric field in the device structure and this further enhance the carrier concentration and spatial confinement of the 2DEG in the channel. Therefore, the AlGaN/GaN HEMTs can achieve a very high values of 2DEG sheet carrier concentration (n_s) of 10^{13} atoms/cm^2 [1.24], without the

requirement of any intentional doping [1.25] in the device structure. In general, the doping could reduce the electron mobility through scattering mechanisms. However, in case of AlGaN/GaN HEMTs, surface scattering is significantly reduced by shifting the current-carrying region below the AlGaN barrier and therefore, the electrons tend to have high mobility and hence the device is referred to as High Electron Mobility Transistor.

It is widely known that built-in electric fields formed due to polarization induced charges in the GaN crystal and this plays a crucial role in determining the electrical and optical properties of GaN-based devices. There are two kinds of polarization namely spontaneous and piezoelectric polarization that contribute to the formation of 2DEG in the AlGaN/GaN HEMT device [1.24]. The spontaneous polarization refers to the built-in polarization field existing in an unstrained GaN crystal. This polarization field exists because the crystal lacks its symmetry and the resulting bond between two atoms is not purely covalent. This results in the displacement of the electron towards one of the atoms in the crystal bond and this cause the accumulation of surface charges of opposite polarity across both the ends of the crystal [1.26]. In an ordinary GaN crystal, the polarization charges do not accumulate because the oppositely charged charges tend to cancel each other. However in case of AlGaN/GaN heterostructure, the GaN crystal suddenly ends and AlGaN crystal begins to grow, so there is an abrupt change at the hetero-junction interface. This contributes to an electrically charged region in the vicinity of the junction. The surface charge formed due to the spontaneous polarization in a Ga-face crystal of GaN and AlGaN grown on c-plane is shown in Fig. 1.2. Fig. 1.3 shows the spontaneous polarization coefficients (P_{sp}) of the group III-V nitride materials [1.26]. The piezoelectric polarization charge is formed due to the presence of a polarization field resulting from the distortion of the crystal lattice.

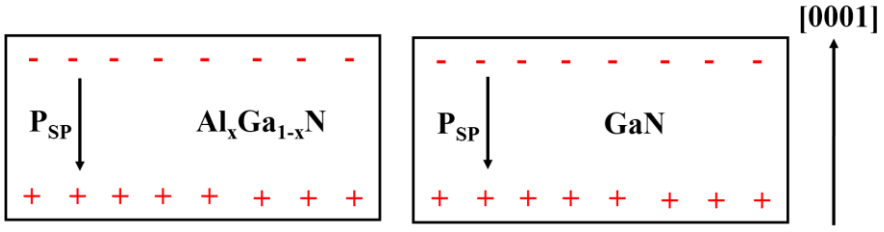


Fig. 1.2. Electric field and polarization charge present due to spontaneous polarization mechanism in GaN and AlGaN crystals grown on c-plane (Ga-face crystal) [1.26].

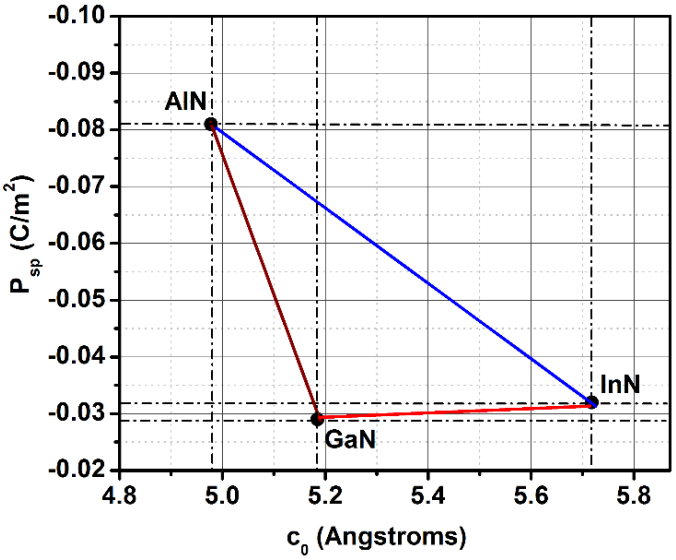
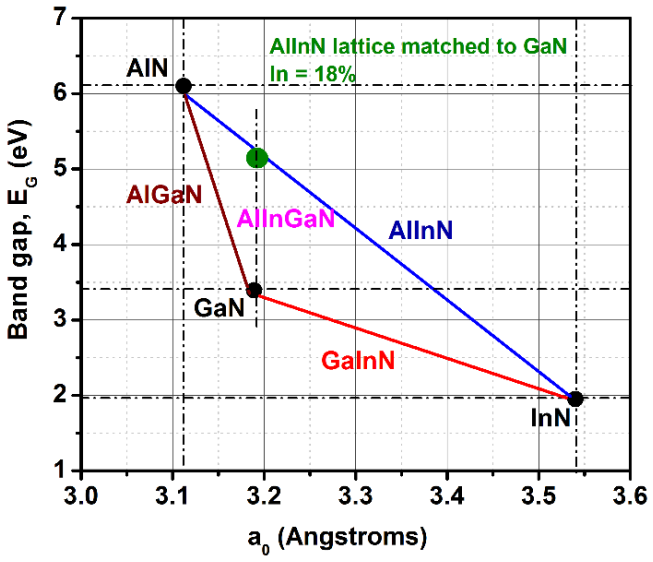
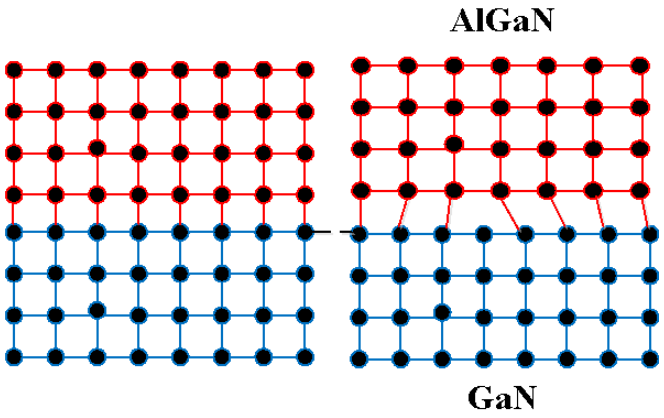


Fig. 1.3. Spontaneous polarization coefficients of group III-V nitrides [26].

The lattice constants of a_0 and c_0 for GaN material are slightly larger than that of AlN material and hence, the thin AlGaN barrier layer grown over the GaN buffer experiences a tensile strain and it is shown in Fig. 1.4. The amount of tensile strain produced is directly proportional to the thickness of the grown AlGaN barrier layer. However, the GaN is normally relaxed due to the thick grown buffer region on the selected substrate. Moreover, in case of the nitride system, the piezoelectric constants are at-least ten times higher than those of typical III-V semiconductors and this results in large polarization field [1.24], [1.26].



(a)



(b)

Fig. 1.4. Strain induced piezoelectric polarization in the AlGaN/GaN heterostructure. (a) Band gap values vs. lattice constant c_0 of group III-V materials. (b) Lattice structure illustrating the tensile strain [1.26].

Fig. 1.5 shows the values of piezoelectric coefficients in GaN and other group III-V nitrides. Therefore, a large magnitude of polarization charges are induced at the hetero-junction interface. Fig. 1.6 shows the electric field and piezoelectric polarization charges existing in a conventional AlGaN/GaN HEMT structure grown on c-plane, in a Ga-face crystal structure. The strain induced due to piezoelectric polarization can alter the band structure and thus changes the sheet carrier concentration in the channel region. Hence, the strain induced polarization provides an additional way of engineering, through which the HEMT device characteristics can be improved.

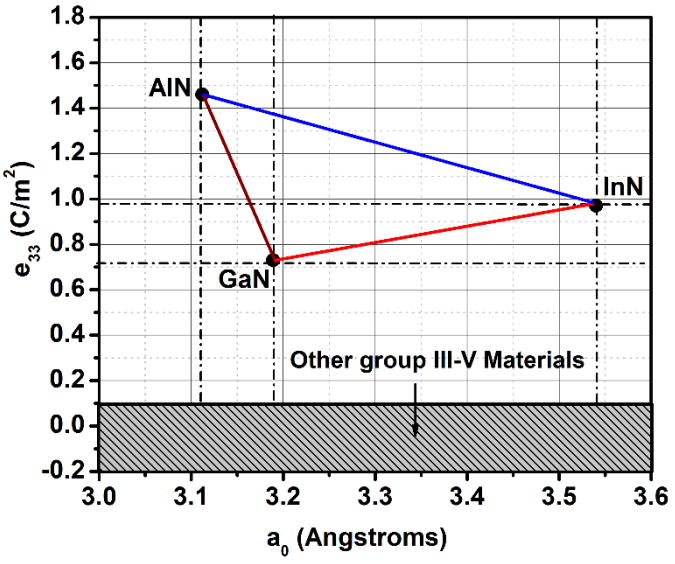


Fig. 1.5. Piezoelectric polarization coefficients of group III-V materials [1.26].

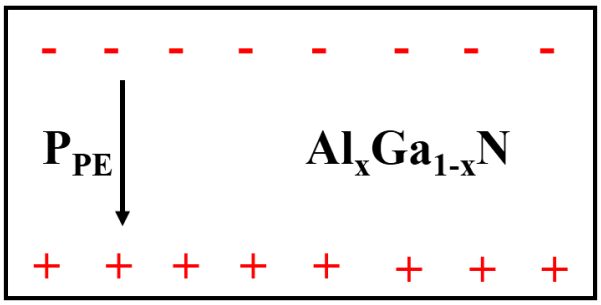


Fig. 1.6. Electric field and polarization charge present due to piezoelectric polarization mechanism in AlGaN crystals grown on c-plane (Ga-face crystal).

Recently, it has been reported that InAlN material with an 18% mole fraction of indium demonstrated an excellent lattice match with the thick GaN buffer and thereby improved the device performances [1.27], [1.28].

A typical cross section of doped AlGaN/GaN HEMT device is shown in Figure 1.7. The two-dimensional electron gas (2DEG) formed at the hetero-junction interface between AlGaN barrier layer and the unintentionally doped GaN layer is highlighted in the figure. The AlGaN spacer layer in the device structure is generally used to separate the doped AlGaN barrier layer from the channel region (hetero-junction interface) and thereby reduces the possibility of impurity scattering to make sure the high electron mobility [1.29]. As the AlGaN spacer layer thicknesses increases, the dopants are separated far away from the channel region which reduces the scattering effects and thus electrons can achieve high mobility.

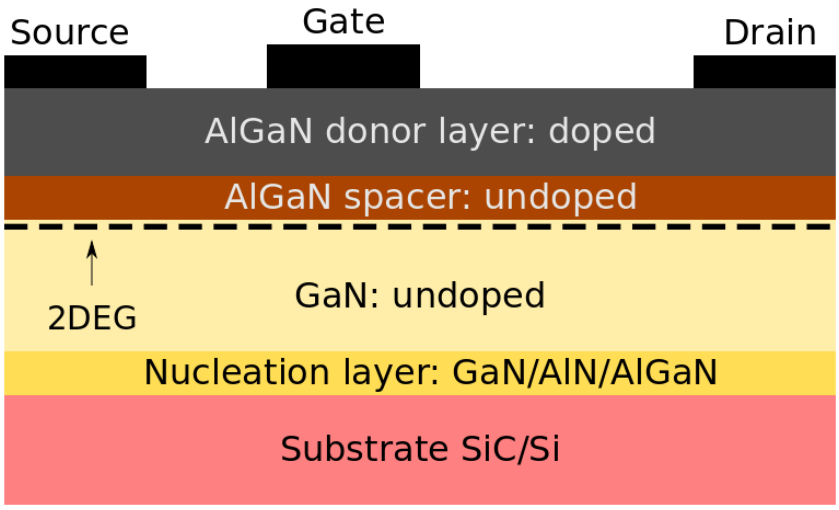


Fig. 1.7. Schematic cross section of conventional AlGaN/GaN HEMT.

In a typical doped AlGaN/GaN HEMT structure, the doped AlGaN barrier layer supplies electrons to the hetero-junction interface. However, intentional doping is not essential for the AlGaN/GaN HEMT devices due to the high polarization charges induced in the device structure, capable of producing a sheet carrier concentration of 10^{13} atoms/cm^2 at the hetero interface region [1.30]. Moreover, the contribution of the doped AlGaN barrier layer to the formation of 2DEG at the hetero interface region has been reported to be less than 10% due to the polarization nature of GaN material [1.30]. It has also been reported that the doped AlGaN/GaN HEMT structures show better DC performance compared to un-doped GaN HEMTs, higher doping in AlGaN barrier layer would results in increased scattering mechanisms and it might degrade the RF performance of the device [1.31]. The barrier layer thickness and the Al mole fraction also play a major role in determining the RF small signal gain performance of the device [1.32]. Ohmic contacts are used for the source and drain regions and the gate region has a Schottky contact. For smaller applied drain-source voltage (V_{DS}), the drain current (I_D) is approximately linear. Moreover, the AlGaN/GaN HEMT is a depletion mode device and hence, a large negative V_{GS} bias is applied to shut down the device and this is possible by implementing the Schottky gate contact on the device. When the negative bias is applied across the gate-source (V_{GS}), the electrons are partially depleted from the 2DEG channel and thereby, increases the resistance. If the applied V_{GS} reaches the threshold voltage (or pinch-off, $V_{pinch\text{-}off}$), the electrons are completely depleted from the channel and therefore, the channel region is closed. The drain current gradually drops to zero and this specific condition is called device pinch-off. Therefore, the Schottky gate contact used in GaN HEMT devices has two major functions (i) depletes the channel (ii) avoids the parasitic parallel conduction (like in MESFET) between the source and drain regions. The source and drain contacts are usually formed using Ti/Al (or) Ti/Au and the Schottky gate contact is made from Ni/Au (or) Pt/Au [1.33].

The typical structure shown in Fig. 1.7 has suffered from major problems such as DC-RF dispersion which is related to surface and bulk traps and high leakage current [1.19], [1.34]. The DC-RF dispersion describes the difference in the output power estimated from DC-IV curves and from the load pull power measurements [1.35], [1.36]. These problems severely limit the operation of GaN HEMT, especially for microwave high power applications. The DC-RF dispersion problem has been reduced by the introduction of SiN passivation [1.37], [1.38] in the device structure and thereby the significant improvement in the output power can be achieved [1.39], [1.40]. Moreover, the SiN passivation also helps to increase the breakdown

voltage of the device [1.39]. The break down voltage can be further increased by implementing the field plate structure for the gate region of the device [1.41]. A field plate is a metal plate, placed over the gate region and extended towards the drain region, in order to sustain the uniform electric field in the device structure, especially at the gate-drain edge and thereby reduces the degradation issues. The field plate also has a significant role in determining the large signal performance of the device.

Two different types of field plate structure can be found in the literature namely the gate and the source connected field plates [1.19], [1.42], [1.43]. The cross section of gate and source connected field plate structure is shown in Figure 1.8. The gate field plate can be constructed either as a part of the gate (or) connected to the gate by an external means. The introduction of gate field plate improves the breakdown voltage of the device but it imposes the additional problem of increased gate-drain feedback capacitance (C_{gd}) and this causes the reduction of small signal power gain and the maximum cut-off frequency of the device [1.43]. Whereas in case of source connected field plate structure, the field plate to channel capacitance contributes to the drain-source capacitance, which avoids the increase of C_{gd} and hence it provides improved small signal gain performance [1.43].

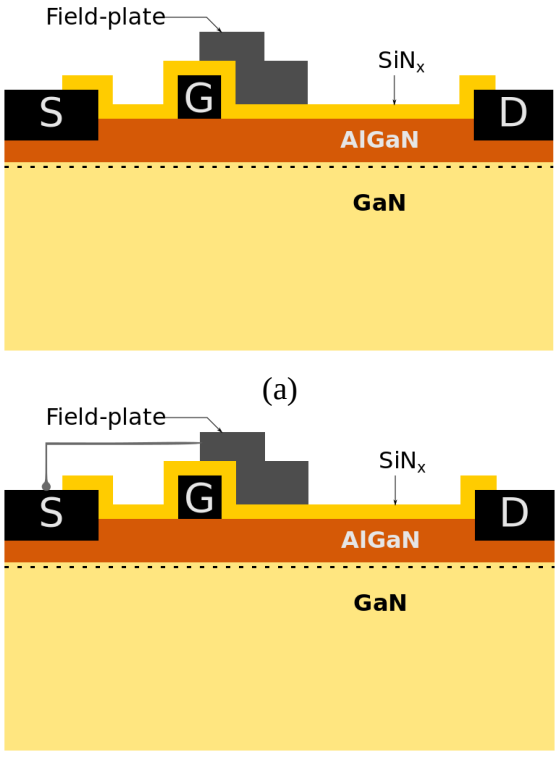


Fig. 1.8. Modified field plate structure of AlGaN/GaN HEMT device (a) gate connected (b) source connected.

1.5. Substrates

The AlGaN/GaN epilayers are widely grown on sapphire, SiC and Si substrate due to the significant cost and complications involved in producing a large amounts of GaN wafers. However, GaN can be the ideal substrate as there would be no lattice mismatch and this would reduce the number of defects generated in the device. Recently, diamond have been considered as another choice due to its high thermal conductivity but still it is expensive to use. One of the major role of the substrate is to conduct and efficiently dissipate the heat generated during the device operation. Table 1.2 gives some important properties of substrate which must be considered while fabricating high frequency electronic devices.

Table 1.2. Summary of different substrate materials properties used for GaN devices.

Substrate	**Thermal conductivity at 300 K (W/ cm. K)**	**Lattice mismatch to GaN (%)**	**Thermal expansion coefficient mismatch (%)**	**Wafer cost**
GaN	1.3	0	0	Very expensive
SiC	4.55	3.5	25	Expensive
Sapphire	0.35	14 – 23	34	Moderate
Si	1.54	17	56	Less expensive

Sapphire

Sapphire is an insulating material with a poor thermal conductivity and it also has the largest lattice mismatch with GaN, compared to other commonly used substrate materials. Depending on the relative orientation with GaN, the lattice mismatch generally varies between 14% and 23%. The large lattice mismatch would cause the large number of defects (10^{10} cm^2) generated in the GaN layers. This lattice mismatch also has influence on reducing the carrier mobility, reducing the life time of minority carriers in the device, decreasing the overall thermal conductivity and all of these effects would degrade the device performance. However, this substrate is economically viable and available in large size wafer diameters. Therefore, GaN-on-sapphire has been the most commonly used substrate over the years, for evaluating the performance capability of GaN-based devices in high frequency applications.

Silicon Carbide (SiC)

SiC is the most suitable substrate for GaN devices, since the lattice mismatch between GaN and SiC material is < 4%. It has the high thermal conductivity (4.55 W/cm. K) which is crucial for high power applications, and also relatively low thermal expansion coefficient (TEC) mismatch. The density of dislocations when the layer of GaN is grown over SiC substrate is under 10^8 cm^{-2}. SiC is generally considered to be the best material for producing powerful electronic devices and also the appealing choice of substrate for commercial GaN RF applications. Unfortunately, SiC substrate is expensive.

Silicon (Si)

Si is probably the most attractive substrate among all others due to the availability of large diameter wafers and low cost. The lattice mismatch between GaN and Si is 17% and the lattice constant is higher than GaN. Therefore, GaN layers grown on Si substrate experience a tensile stress, which leads to generation of crystal defects and dislocations, degrades the performance of the device. However, Si material has a moderate thermal conductivity of 1.54 W/cm K. In recent years, a significant amount of work has been devoted to the development of GaN-on-Si substrate. The state-of-the-art has also been reported for the AlGaN/GaN HEMT devices grown on Si substrate in [1.13], [1.14].

1.6. Choice of Buffer Configuration

The electrical properties of the GaN buffer layer is significantly important for the realization of high efficient GaN HEMT devices [1.44]. The presence of deep levels in this highly resistive buffer layer are a necessary requirement to reduce the leakage current and also the short-channel effects [1.44] [1.45]. Such deep levels can be due to either intrinsic defects or by introducing external dopants such as iron (Fe) or carbon (C) [1.45]. However, the high density of defects in the buffer induces the trapping mechanism [ref] and are strongly correlated with the device operation. The iron doping in the GaN buffer result in Fermi level pinned to the upper half of the bandgap whereas the carbon doping pin the Fermi level in the lower half and thereby, causing significant current-collapse [1.45]. As a suitable alternative, the AlGaN back barrier double hetero-junction devices have been considered recently, and they demonstrate high electron confinement, high frequency performance and low trapping effects [1.46]. However, the presence of AlGaN back barrier has a negative impact on the thermal performance. Moreover, the thermal conductivity of the back barrier decreases with increase in Al mole fraction and thus, results in poor device performance [1.46]. Furthermore, higher gate leakage

current is commonly observed in AlN/GaN/AlGaN HEMT back barrier devices. Therefore, selecting a suitable buffer configuration plays a vital role in obtaining desired device performance from GaN HEMT technology.

1.7. Key Challenges of GaN HEMT Technology

Although GaN HEMT devices have demonstrated the state-of-the-art performance for RF and microwave power applications. Trapping effects are one of the major factor that limits the performance of AlGaN/GaN HEMT devices till today [1.30]. The presence of material defects due to the growth of AlGaN/GaN epilayers on a lattice mismatched substrate, or the distortion of crystal lattice due to the formation of hetero-junction interface, create deep levels inside the device that act as traps for charge carriers. Fig. 1.9 shows the possible location of traps in the AlGaN/GaN HEMT devices. The parasitic charges moving in and out of these traps located on different regions of the device degrade the device dynamic performance and also their reliability [1.47]. The different locations of traps inside the device causes different parasitic effects that degrade the DC performances, dynamic transconductance, on-resistance (R_{ON}) or the RF output power [1.47], [1.48]. Furthermore, it is important to note that the definite correspondence between the parasitic effect and the associated location of traps inside the device is not well completely understood. However, many papers reported in the literature by several research groups show consistent results relating the parasitic effect along with its physical location of traps in the device.

The following sub-sections describe the commonly observed parasitic effects in the GaN-HEMT devices and its influence on the device performance.

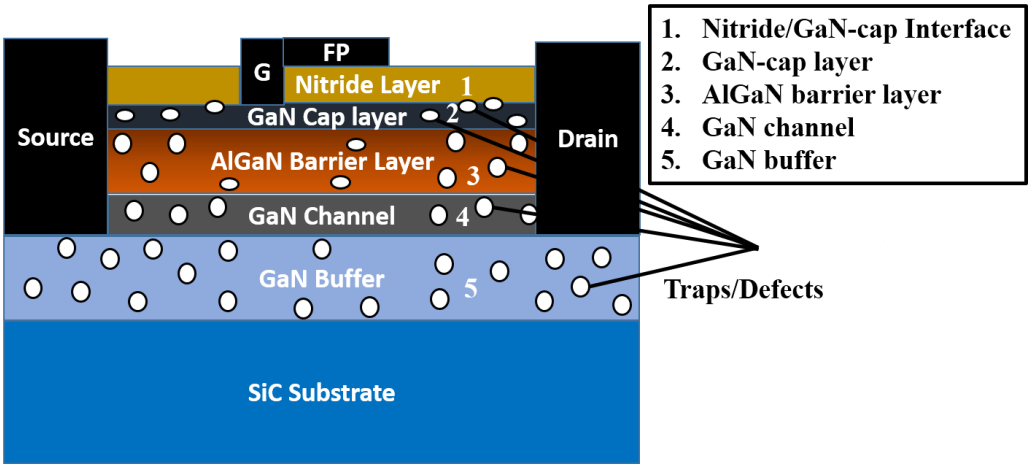


Fig. 1.9. Schematic cross section of GaN/AlGaN/GaN HEMT device describing the possible physical location of traps.

1.7.1. Current Collapse

Current collapse is the widely reported parasitic effect in GaN HEMTs that causes the significant reduction of output power at high frequency. The current collapse has also been referred as current slump, DC/RF dispersion or current compression [1.26], [1.34]. It is basically the discrepancy observed between the DC and RF measured output power of the device. It causes a reduction of the dynamic saturation drain current compared to the DC-ones and therefore, increases the access resistance. This also results in reduction of the device dynamic transconductance, increase of knee-voltage (V_{Knee}) and further, leads to reduction of RF gain and the measured output RF power [1.34], [1.36]. Moreover, the current collapse also increases the high-frequency distortion and reduces the efficiency. The current collapse can be described using the following equation [1.26]:

$$P_{out} = \frac{1}{8} * I_{DS,max} * \left(V_{Breakdown} - V_{Knee}\right) \tag{1.1}$$

Where $I_{DS,max}$ and $V_{Breakdown}$ are the measured maximum drain current and breakdown voltage of the device at DC conditions, respectively.

To explain the lower RF output power, $I_{DS,max}$ is supposed to decrease whereas V_{Knee} will be increased, compared to the measured DC values and this has been illustrated in Fig. 1.10. This parasitic effect is correlated with the existence of traps in the device. Although traps can be located in the buffer layer or the barrier layer or at the surface of the device, several research studies suggest that surface traps cause much of the dispersion observed in measurement [1.30]. However, it has been reported in [1.45] that current collapse occurs also due to bulk traps in the buffer region.

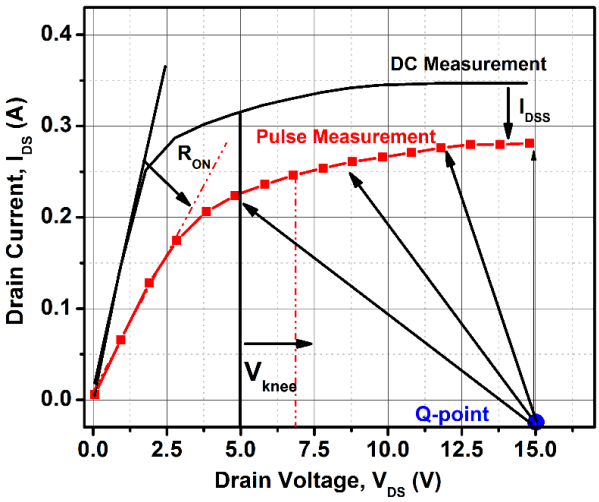


Fig. 1.10. Theoretical representation of current collapse mechanism**.**

The phenomenon of current collapse due to the surface traps can be described using the concept of the virtual gate model [1.26]. Fig. 1.11 shows the schematic explanation of the current collapse trapping mechanism. When the negative gate bias voltage (region I) i.e. below pinch-off voltage is applied to the gate, the high electric field is induced in the device, typically the peak value is located at the drain side edge of the gate.

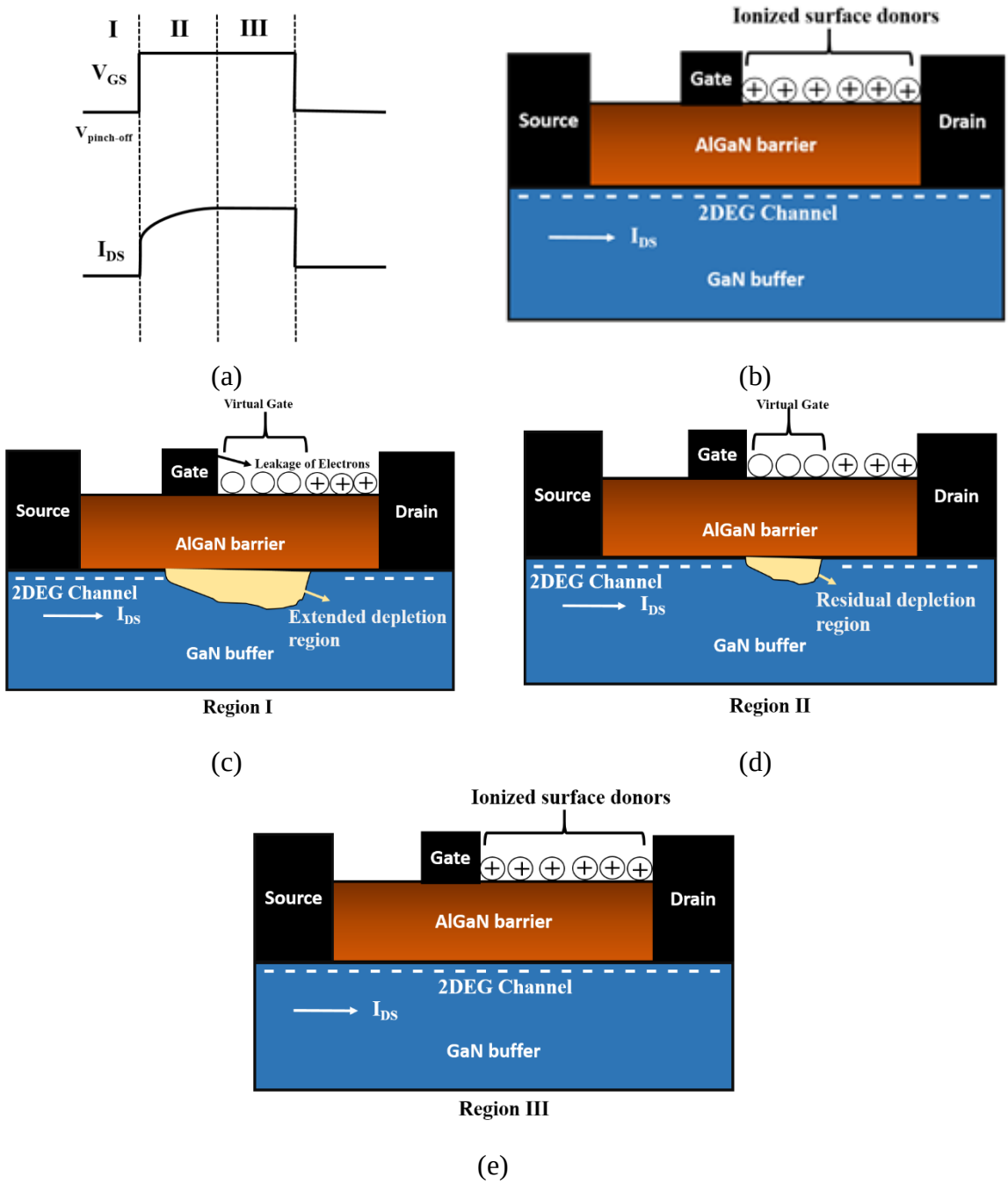


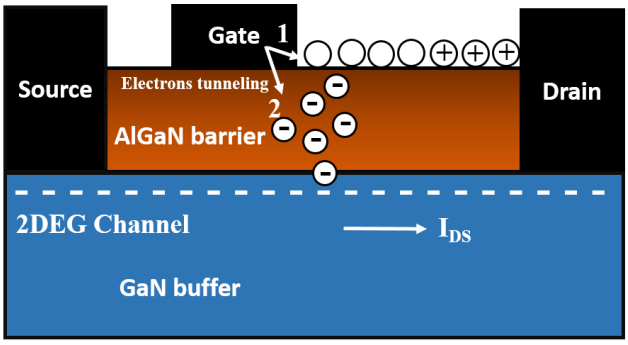
Fig. 1.11. Schematic representation of current collapse mechanism. Timing waveform illustrating the different regions of device operation (a)**,** Zero-biasing conditions (b), Traps behavior when the voltage below device pinch-off (c) and positive bias (d) are applied to the gate and once the device is completely turned-on (e).

This results in leakage of electrons between the gate and drain and, can fill the ionized donor states located on the surface close to the gate terminal of the device. It is important to note that these positively charged ionized donors (surface donors) are essential to balance the electrons (2DEG) existing in the potential well. Therefore, the charging of ionized surface donors, forces the surface potential to become negative and as a consequence, the channel under the part of the drain access region next to the gate terminal is completely depleted out of electrons. The extended depletion region due to the negative surface potential that acts as negative biased virtual gate is shown in Fig. 1.11 (c). Therefore, under this condition, the current along the channel is controlled by two gates: the usual gate terminal, controlled by the applied external gate bias voltage, and the virtual gate, controlled by amount of charges trapped on the surface. In region II, the gate bias is assumed to be positive, the channel under the gate turns-on immediately, and however, the virtual gate controlling the channel under the drain access region is slow to respond (Fig. 1.11 (d)). The amount of delay in responding to the applied gate bias strongly depends on the de-trapping transient of the surface traps. The deep level traps and the low electron mobility values under this region are responsible for the degradation of drain current. Although, the gate bias is changed to positive, the drain access region is still depleted out of electrons and hence, possesses a low carrier concentration. This induces a highly resistive drain access region and most of the applied potential drops across this region and therefore, the drain current remains low. However, the captured electrons are eventually emitted from the traps after some period of time (region III) and thereby, the drain current reaches the steady state value (Fig. 1.11 (e)). Therefore, for high frequency operation, if the electric field is sufficiently high to fill the surface traps, the device operation strongly depends on the obtained maximum drain current, considering the slowest phenomena between the RF sweep and the trapping/de-trapping transients of these surface traps and not based on the maximum obtainable DC performances [1.26]. In pulsed operation, the device operation is significantly influenced by the trapping effects depending on the applied quiescent bias point, and by the de-trapping transient obtained after the turning on-pulse. The current collapse phenomenon can significantly degrade not only the dynamic RF performance of the devices, but also the high-power switching applications. The increase in the drain access resistance and knee voltage can considerably increase the power dissipation even under switch-OFF conditions. Therefore, to minimize the current collapse mechanism, different techniques such as surface passivation and the adoption of field-plates have been reported in the literature [1.39], [1.41]. The surface passivation creates an optimal dielectric-semiconductor interface that prevents the filling of ionized surface traps by the electrons leaking from the gate and hence, reduces the current collapse mechanism. The

field-plate in the device structure allows the lateral distribution of electric field over the drain access region and thereby, preventing the peak electric field located near the drain side of the gate edge. This will limit the electron trapping and emission process and hence, prevents the increase of the current collapse effect.

1.7.2. Gate-Lag

The gate-lag is used to describe the slow transient response observed in the drain current measurement when the applied gate voltage of the device is changed abruptly. The gate-lag is observed due to two physical mechanisms. The first one is related to the presence of ionized surface state donors over the un-gated surface of the device. The high reverse bias voltage applied to the gate terminal causes the leakage of electrons between the drain side gate edge and drain access region and the surface ionized donors capture these electrons, results in the increased depletion region of the channel. This effect has been modeled as a virtual gate as explained in the previous section. The second one is related to the positive shift of pinch-off voltage of the device due to the charge trapping process under the gate [1.49]. These traps are located in the AlGaN barrier or the GaN layers. Fig. 1.12 shows the schematic representation of gate-lag mechanism. Moreover, it has been reported in [1.49], AlGaN/GaN HEMT with Ion Tin Oxide (ITO) gate confirms the existence of traps under the gate region because of the higher gate leakage component in the device. The higher gate leakage current in the device injects necessary electrons for charging the trap states located under the gate during the application of reverse biased gate voltage. The use of passivation layer and the implementation of field plate at the gate can reduce the gate-lag effects [1.30].



1. Surface trapping
2. Trapping under the gate

Fig. 1.12. Schematic description of gate-lag mechanism. Two possible mechanisms (i) surface trapping and (ii) trapping under the gate.

Fig. 1.13 shows the gate-lag measurements of GaN/AlGaN/GaN HEMT grown on SiC substrate with the gate length (L_G) of 0.25-µm and gate width (W_G) of 600-µm (eight fingers, n=8), respectively.

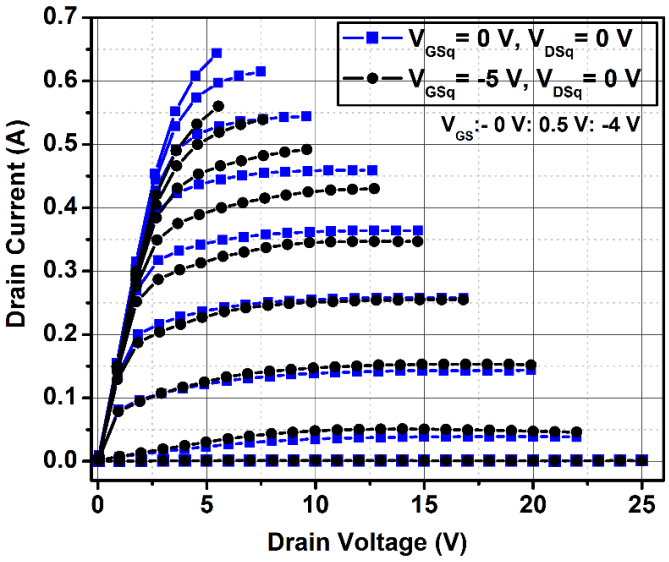


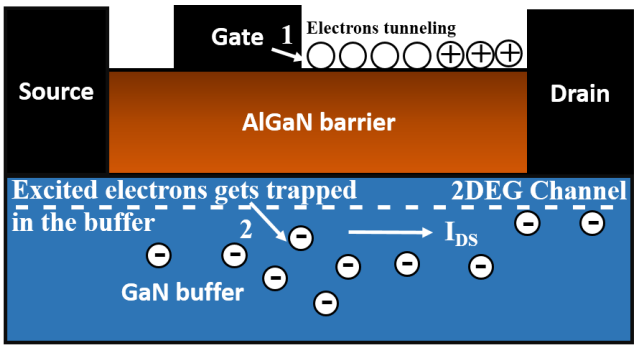
Fig. 1.13. Measured pulsed I-V characteristics of the GaN/AlGaN/GaN HEMT device grown on SiC substrate illustrating the gate-lag effect.

The device pulsed I-V characteristics have been measured under two biasing conditions: one at V_{GSq}, V_{DSq} = (0 V, 0 V) and the other at V_{GSq}, V_{DSq} = (-5 V, 0 V). The pulse width and pulse period applied to the drain terminal are 900-ns and 900-µs, respectively. Pulsing the device from steady state biasing conditions (0 V, 0 V) results in an ideal I-V characteristics, however, a drastic reduction in drain current due to gate-lag mechanism is observed under (-5 V, 0 V) biasing conditions.

1.7.3. Drain-Lag

The term drain-lag is used to describe the slow transient observed in drain current measurement when the applied drain voltage of the device is pulsed abruptly and a high negative bias (below $V_{pinch\text{-}off}$) is applied to the gate terminal of the device. Therefore, drain-lag effect is the combined response of the applied gate and drain biasing conditions. Fig. 1.14 shows the schematic explanation of drain-lag mechanism observed in GaN HEMTs. A very high negative bias applied to the device induces the gate-lag effect due to the leakage of electrons on the surface of the device and this modulates the electrons available in the 2DEG channel. Moreover, pulsing the drain terminal to a higher biasing conditions results in an increased electric field across the device. Fig. 1.15 shows the drain-lag measurements of GaN/AlGaN/GaN HEMT grown on SiC substrate under the same conditions as shown in Fig. 1.13. The pulsed I-V characteristics have

been measured under two biasing conditions: one at V_{GSq}, V_{DSq} = (-5 V, 0 V) and the other at V_{GSq}, V_{DSq} = (-5 V, 15 V), to show the influence of drain-lag effects. Therefore, the electrons in the channel gets excited due to the applied higher drain biasing conditions and those excited electrons can escape from the channel and gets trapped in the buffer region of the device [1.30], and thereby causes the significant reduction of drain current.



1. Surface trapping
2. Trapping in the buffer

Fig. 1.14. Schematic representation of drain-lag mechanism. High negative bias applied to the gate cause tunneling of electrons from gate to the surface and high drain bias cause the excitation of channel electrons and those electrons could easily get trapped in the buffer.

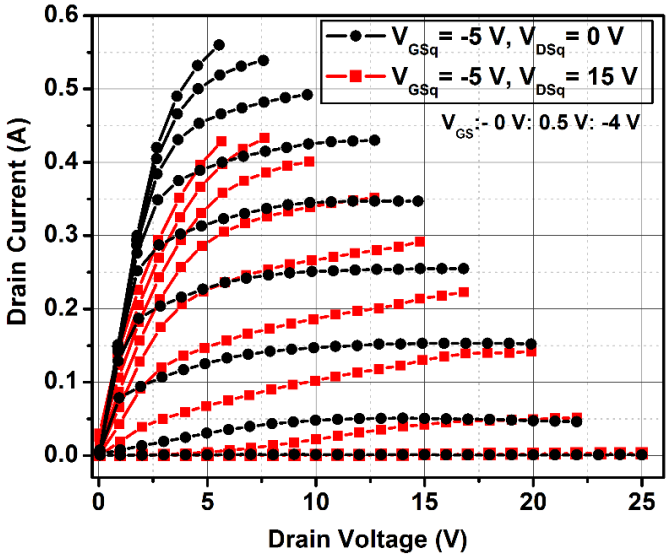


Fig. 1.15. Measured pulsed I-V characteristics of the GaN/AlGaN/GaN HEMT device grown on SiC substrate illustrating the drain-lag effect.

1.8. Reliability Issues

Although the GaN HEMT device excellent performances have been widely reported, the reliability issues still persist and this limits the commercialization of these devices. The

following sub-sections discuss the important degradation device mechanisms which affects the reliability of GaN HEMTs.

1.8.1. Self-Heating and Hot-Electrons Degradation Effect

Self-heating (SHE) and hot-electrons effects [1.50]–[1.52] are the major issues that are strongly correlated and adversely affect the device performance and its reliability. The high power density and large breakdown electric field allows device operation even with the concurrent existence of very high electric field and high density of electrons in the channel. The applied high biasing conditions induce the high electric field in the device structure and particularly, the peak electric field is located at the drain side gate edge. Fig. 1.16 shows the schematic cross section of AlGaN/GaN HEMT device describing the high electric field region. The high electric field results in large amount of heat generated as well as a large current in the channel region of the device. Therefore, the electrons flowing in the channel acquires high energy and becomes hot carriers [1.53]. These hot carriers travel in an in-elastic mean free path of the channel region before they transfer the acquired high energy to the crystal lattice and hence, the channel temperature increases drastically, in turn accelerates the phonon scattering [1.50]. This will degrade the carrier mobility and thereby, the drain current. The negative slope observed in the drain current characteristics is due to the self-heating effect [1.50].

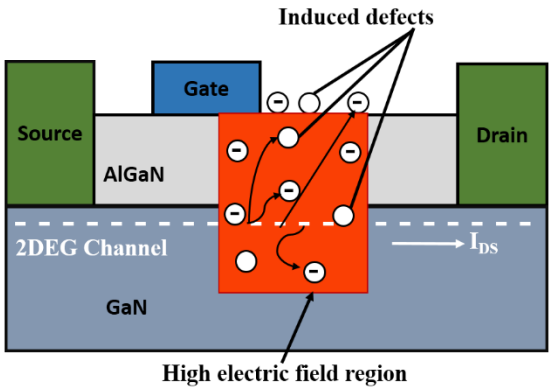


Fig. 1.16. Schematic cross section of AlGaN/GaN HEMT describing the high electric field region. The hot electrons create defects in the different device layers and capture the electrons.

The hot electrons generation in the channel is particularly important for sub-micron gate length devices. These hot electrons can easily overcome energy barriers, can transfer the acquired high energy by colliding with the crystal lattice and they can create defects or dangling bonds inside the device layers which act as traps for charge carriers. The traps can be either generated in the channel, in the barrier or at the interface regions, depending on the kinetic energy of the hot

electrons. In addition, the electrons may directly tunnel from the channel to the gate or to the AlGaN barrier or GaN buffer, may get captured in preexisting traps inside the device [1.50]. Therefore, this process partially depletes the 2DEG channel and leads to degradation of drain current. The main consequences of hot electrons degradation effect are the shift of pinch-off voltage, reduction of transconductance and the increase of on-resistance of the device [1.50], [1.52].

In GaAs HEMTs, the hot electron induced degradation can be identified by monitoring the increase in gate leakage current, caused by the collection of holes generated by impact-ionization process [1.52]. However, in GaN HEMT devices, the impact-ionization rate is considered to be negligible and the gate leakage current is generally controlled by the electron tunneling process (tunneling through AlGaN barrier). Therefore, the hot electron degradation effect in GaN HEMTs is usually characterized using electroluminescence (EL) measurements [1.54] .

1.8.2. Gate-Edge Degradation

When the GaN HEMT device is operated in the off-state, the gate-drain Schottky junction is degraded due to the applied reverse biasing conditions and this mechanism is referred to as gate-edge degradation. The higher reverse biasing applied to the gate-drain Schottky junction induces the high electric field in the device, thus enhancing the tensile strain and the stored elastic energy (converse piezoelectric effect) of the gate-drain access region [1.55], [1.56]. Once a critical value of tensile strain or elastic energy is reached at the drain side gate-edge, this stress is relaxed through the formation of crystallographic defects in the AlGaN barrier region. This promotes the injection of electrons from the gate metal into the AlGaN barrier, through a trap-assisted tunneling mechanism, creating parasitic paths for the leakage current to flow. It results in the increase of gate leakage current in the device and also contributes to other trapping related effects. The major consequences of the gate-edge degradation effect are the increase of gate leakage current, worsening of current collapse, increase of parasitic drain (source) resistance and a decrease of saturated DC drain current (I_{DSS}). The gate-edge degradation can be investigated through several measurement techniques such as Transmission Electron Microscopy analysis (TEM), Electroluminescence microscopy and Destructive Physical Analysis (DPA) [1.56].

1.9. Gate Leakage

Gate leakage is one of the major issue that affects the performance of GaN HEMT devices. It refers to leakage of current through the gate by electron tunneling process which degrades the RF and noise performance of the device [1.57]–[1.59]. The 2DEG channel of the GaN HEMT device is controlled by the Schottky gate contact and higher negative bias is generally applied to turn-off the device. Therefore, the gate leakage becomes significantly important in determining the performance and reliability of these devices. An extensive research has been conducted to analyze the temperature and bias dependencies of gate leakage in AlGaN/GaN HEMT devices [1.60]–[1.62]. It has been suggested that Poole-Frenkel (PF) emission is considered to be the dominant mechanism responsible for higher gate leakage at higher operating temperatures. However, Fowler-Nordheim (FN) tunneling is also been observed at very low operating temperatures [1.62]. Moreover, the bias dependence gate leakage can be described using thermionic emission and trap-assisted tunneling mechanisms [1.63].

1.9.1. Thermionic Emission Model

In forward bias, the gate leakage at the Schottky junction is predominantly due to thermionic emission (TE). Fig. 1.17 shows the conduction band diagram of metal/AlGaN interface illustrating the thermionic emission process.

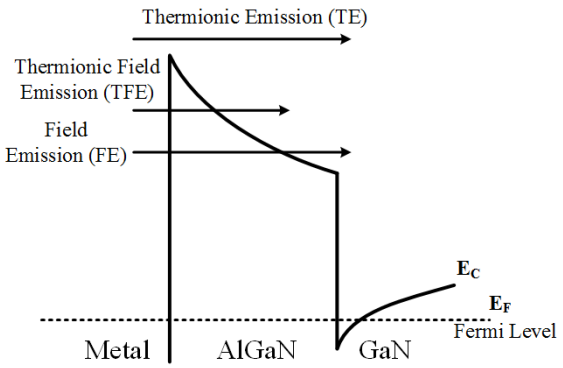


Fig. 1.17. Gate leakage mechanism – Thermionic Emission.

The current density-voltage characteristics of a Schottky gate junction is given by [1.63]:

$$J_{TE} = J_{TE0}\left[\exp\left(\frac{V}{\eta V_{th}}\right) - 1\right] \tag{1.2}$$

$$J_{TE0} = A^{*}T^{2}\exp\left(-\frac{\phi_b}{V_{th}}\right) \tag{1.3}$$

where J_{TE0} is the reverse saturation current density, A^* is the effective Richardson's constant, T is the absolute temperature, ϕ_b is the Schottky barrier height, V is the applied potential, η is the ideality factor and V_{th} is the thermal voltage, respectively.

1.9.2. Poole-Frenkel Emission Model

The reverse gate leakage current of GaN HEMT devices is significantly higher than that predicted by thermionic emission model. It is due to the existence of traps in the device and it plays an important role in determining the gate leakage component of these devices [1.58]. In the low reverse gate bias region, the current conduction is due to Poole-Frenkel (PF) emission. The electric field enhanced thermal emission of electrons from the traps state to the continuum of states formed by the conductive dislocations existing in the AlGaN barrier is responsible for PF emission [1.62]. Fig. 1.18 shows the classical conduction band diagram and the continuum states describing the physical mechanism of PF emission. The trap states are assumed to be located very close to the metal Fermi level and the continuum of states (E_{dis}) formed due to the conductive dislocations in the AlGaN barrier, is at a height ϕ_t from the gate metal Fermi level. The increasing gate voltage (V_g) increases the electric field in the device and correspondingly, increases the current due to the reduction in barrier height for electron emission. Moreover, the increase in temperature results in increased current owing to the higher thermal energy acquired by the charge carriers to jump from trap state to the conductive dislocations in the AlGaN barrier. Therefore, the PF mechanism dominates the gate leakage current in the low to medium reverse-bias region.

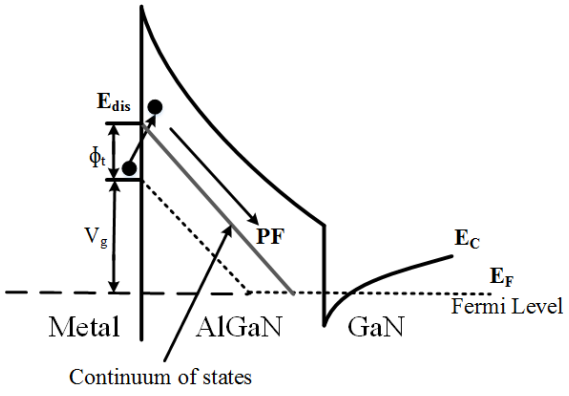


Fig. 1.18. Gate leakage mechanism – Poole-Frenkel Emission.

The relation between current density (J_{PF}) and electric field (E) for PF mechanism is described by [1.63]:

$$J_{PF} = C.E.\exp\left(\alpha + \beta\sqrt{E}\right) \tag{1.4}$$

with: $\alpha = -\phi_t/V_{th}$ and $\beta = (q/\pi\varepsilon_s)^{1/2}/V_{th}$.

C is the parameter dependent on the concentration of traps, ϕ_t is the barrier height for the electron emission from the trap state to the dislocation and ε_s is the dielectric permittivity of the semiconductor, respectively.

The electric field at the metal-AlGaN barrier can be computed using (1.5) [1.62]:

$$E = \frac{q(\sigma_b - n_s)}{\varepsilon} \tag{1.5}$$

where σ_b is the sum of the piezoelectric polarization charge in the AlGaN barrier and the difference between spontaneous polarization charge in the barrier and the GaN buffer, n_s is the 2DEG concentration at the AlGaN/GaN hetero-junction interface and ε is the dielectric permittivity of the AlGaN material.

1.9.3. Fowler-Nordheim (FN) Tunneling Model

If the high reverse bias is applied to the gate, the electric field across the AlGaN barrier increases drastically and this results in thinning of the barrier height at the metal Fermi level. Therefore, it facilitates the carriers to tunnel across the triangular barrier as shown in Fig. 1.19. The increase in electric field reduces the tunneling barrier width and causes the increasing FN tunneling leakage current. However, this process must be independent of temperature.

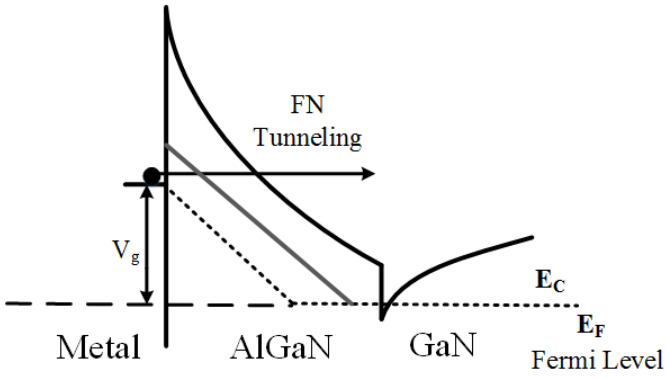


Fig. 1.19. Gate leakage mechanism – Fowler Nordheim Tunneling.

The relation between current density and electric field for FN tunneling mechanism is expressed using (1.6) [1.62]:

$$J_{FN} = A.E^2.\exp\left[-\frac{B}{E}\right] \tag{1.6}$$

$$B = \frac{8\pi\sqrt{2m_n^*(q\phi_{eff})^3}}{3qh} \tag{1.7}$$

where *A* is the constant, m^*_n is the conduction band effective mass in semiconductor, ϕ_{eff} is the effective barrier height and *h* is the Planck's constant.

1.9.4. Trap-Assisted Tunneling (TAT) Model

In low-reverse gate bias region, TAT becomes important since it compensates the non-zero PF current at zero gate-biasing conditions. In general, the electric field across the AlGaN barrier saturates for voltages well below pinch-off voltage of the device when 2DEG sheet carrier concentration n_s becomes negligible compared to σ_b [1.62]. The electric field across the barrier is not zero at zero gate-biasing conditions due to the fact that polarization charge is higher than n_s. Therefore, the current flows from gate to the channel through a trap-assisted tunneling (Fig. 1.20) to compensate for the PF emission current flowing from the channel to the gate near zero bias. Moreover, it is demonstrated that trap-assisted tunneling has the same temperature dependence as PF emission.

Therefore, the current density for trap-assisted tunneling mechanism is given by (1.8) [1.62]:

$$J_{TAT} = J_{TAT0}\left[\exp\left(\frac{(V - V_0)}{\eta_2 V_{th}}\right) - 1\right] \tag{1.8}$$

where J_{TAT0} is the reverse saturation current density, η_2 is the ideality factor, V is the applied potential and V_0 is the fitting parameter, respectively.

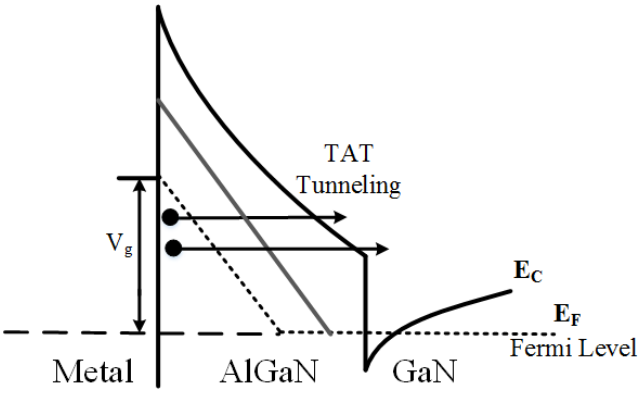


Fig. 1.20. Gate leakage mechanism – Trap-Assisted Tunneling.

1.10. Summary

In this chapter, a brief introduction of the importance of AlGaN/GaN HEMT device technology compared to other existing device technologies has been described. The superior material properties of GaN material and its significance for commercial applications have been explained. The structure of conventional AlGaN/GaN HEMT device, its operation and the implementation of field-plates in the device structure for improving the RF performance have been discussed in detail. Furthermore, the key challenges and reliability issues of GaN HEMT devices such as current collapse, gate-lag, drain-lag, self-heating and hot electrons effects and

gate-edge degradation have been described. The description of gate-leakage current and the different physical mechanisms responsible for the observed gate-leakage have been explained.

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Chapter 2

Physics Based Analytical Device Modeling and TCAD Physical Simulations of AlGaN/GaN HEMTs

Based on Publication:

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Chapter 2. Physics Based Analytical Device Modeling and TCAD Physical Simulations of AlGaN/GaN HEMTs

2.1. Analytical Device Modeling

2.1.1. Introduction

The AlGaN/GaN HEMT has emerged as the most deserving candidate for high temperature, high power and high speed electronic circuits for microwave and mm-wave applications [2.1], [2.2]. This is due to the superior material properties of GaN such as wide bandgap, high thermal conductivity, high saturation velocity and large breakdown field [2.1], [2.3]. The AlGaN/GaN HEMT heterostructure device possesses superior electron transport properties due to the presence of high sheet carrier density at the heterojunction interface produced by the built-in polarization electric field [2.4]. The two-dimensional electron gas density (2DEG) achieved in the GaN HEMT device is well above 10^{13} cm^{-2} [2.5], [2.6], without the requirement of any intentional doping in the device [2.6]. The presence of spontaneous and piezoelectric polarization charges are responsible for such high value of 2DEG sheet carrier density. Furthermore, the increase of Al mole fraction in the AlGaN material will deepen the quantum well and hence facilitate more electrons to be confined in the channel. Therefore, the polarization charge density and bandgap discontinuity can be controlled using the Al mole fraction. This offers the flexibility of optimizing the HEMT device characteristics [2.7].

The progress of AlGaN/GaN HEMT has been quite impressive over the years and nowadays it is widely used in practical applications. Therefore, an accurate model of this device is highly desirable. The numerical calculation of the device characteristics is possible by self-consistently solving (2.4) and (2.6). However, the simulation takes a long time and it is difficult to integrate with modern circuit simulators. Therefore, it is advantageous to develop an analytical model which can be integrated with circuit simulators. Some analytical models of this device have been already reported in the literature [2.7]–[2.11]. These models are rather complex as they often require the calculation of the Fermi level [2.7] for each region of device operation and thus the sheet carrier density is obtained with a suitable approximation.

In this section, we have formulated a simple analytical model of current-voltage characteristics of AlGaN/GaN HEMTs, valid for both intrinsic and extrinsic device. The proposed model accounts the polarization charge density in estimating the 2DEG sheet carrier density. The influence of Al mole fraction and AlGaN barrier thickness in determining the pinch-off voltage

variation and current characteristics is discussed in detail. The effect of source and drain parasitic resistances have also been incorporated to accurately predict the extrinsic HEMT characteristics.

2.1.2. Analytical Model Formulation

A cross-sectional view of the AlGaN/GaN HEMT structure used for modeling is shown in Fig. 2.1. In general, the HEMT structure consists of two layers in which the material with wider bandgap is doped and the material with narrow bandgap energy is normally un-doped. The principle of HEMT operation involves the transfer of electrons from ionized donors into a narrow bandgap energy material to form a conducting layer [2.7]. The transfer of electrons takes place owing to difference in electron affinity values of the two material. The potential well formed at the hetero-junction interface is narrow enough to accommodate the accumulated electrons. The high value of 2DEG sheet density obtained in a HEMT device, cannot be attributed only to the bandgap discontinuity but it is dominantly determined by the polarization electric fields at the hetero-interface. The spontaneous and piezoelectric coefficients of the GaN material are generally quite high, which is an added advantage. The total polarization charge density ($\sigma(m)$) as a function of Al mole fraction (m) at the hetero-junction interface is given by [2.7]:

$$\sigma(m) = P_{sp}(Al_mGa_{1-m}N) - P_{sp}(GaN) + P_{pz}(Al_mGa_{1-m}N) - P_{pz}(GaN) \quad (2.1)$$

The GaN material is considered to be fully relaxed and thus the piezoelectric polarization is zero. Therefore, the total polarization component of GaN contains only the spontaneous polarization. The strain induced piezoelectric polarization of $Al_mGa_{1-m}N$ along the [001] direction can be specified by [2.7]:

$$P_{pz\_AlGaN(m)} = 2\xi_{xy}\left[e_{31}(m) - \frac{c_{13}(m)}{c_{33}(m)}e_{33}(m)\right] \quad (2.2)$$

Where:

$$\xi_{xy} = \frac{a(0) - a(m)}{a(m)} \quad (2.3)$$

and ξ_{xy} is the strain in the x-y plane, $a(0)$ and $a(m)$ are the lattice constants, $e_{31}(m)$ and $e_{33}(m)$ are piezoelectric constants and $c_{13}(m)$ and $c_{33}(m)$ are elastic constants, respectively.

The Al mole fraction dependent parameters of AlGaN material used for analytical model calculation are listed in Table 2.1.

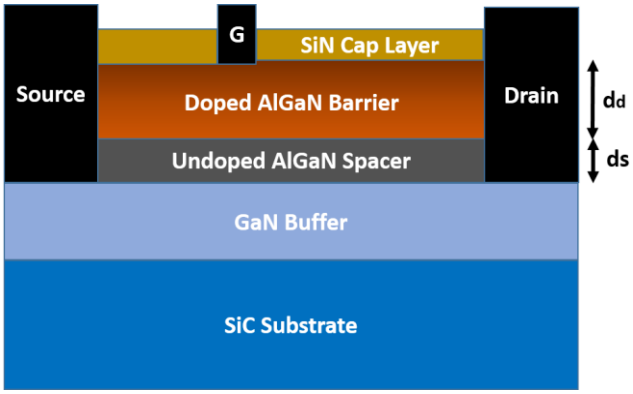


Fig. 2.1. Cross section of an AlGaN/GaN HEMT.

Table 2.1. Aluminum mole fraction dependent parameters of AlGaN for estimating polarization charge [2.6].

Parameter	Expression	Unit
$\varepsilon(m)$	$(-0.5m + 9.5) \times 8.854 \times 10^{-12}$	$cm^{-1}\ V^{-1}$
$\Delta E_c(m)$	$0.7(\{6.13m + 3.42\ (1-m) - m(1-m)\} - 3.42)$	eV
$\Phi_m(m)$	$1.3m + 0.84$	eV
$c_{13}(m)$	$5m + 103$	GPa
$c_{33}(m)$	$-32m + 405$	GPa
$a(m)$	$(-0.077m + 3.189) \times 10^{-10}$	m
$e_{13}(m)$	$(-0.11m - 0.49)$	cm^{-2}
$e_{33}(m)$	$(0.73 + 0.73)$	cm^{-2}
$P_{sp}(AlGaN)$	$(-0.052m - 0.029)$	cm^{-2}

2.1.2.1. Modeling of Sheet Carrier Concentration (n_s)

The 2DEG sheet carrier density can be calculated from the solution of Schrodinger's and Poisson's equations in the quantum well, considering the first two sub-bands in the GaN conduction band. A self-consistent solution of n_s can be expressed as [2.12]:

$$n_s = DV_t \ln\left\{\left[1+\exp\left[\frac{(E_F - E_0)}{V_t}\right]\right]\left[1+\exp\left[\frac{(E_F - E_1)}{V_t}\right]\right]\right\} \quad (2.4)$$

$$E_0 = \gamma_0 n_s^{2/3}, E_1 = \gamma_1 n_s^{2/3} \quad (2.5)$$

$$n_s = \frac{\varepsilon(m)}{q(d_d + d_s)}\left[V_G - V_{OFF}(m) - V(x) - E_F\right] \quad (2.6)$$

where D is the density of states, V_t is the thermal voltage, $V_{OFF}(m)$ is the polarization dependent pinch-off voltage and is given by,

$$V_{OFF}(m) = \Phi_m(m) - \Delta E_C(m) - \frac{qN_D d_d^2}{2\varepsilon(m)} - \frac{\sigma(m)}{\varepsilon(m)}(d_d + d_s) \quad (2.7)$$

Here, $\varepsilon(m)$ is the dielectric permittivity of AlGaN, d_d and d_s are the thickness of doped AlGaN barrier layer and un-doped AlGaN spacer layer, respectively. $V(x)$ is the channel potential at a distance 'x' from the source end of the channel, $\Phi_m(m)$ is the Schottky barrier height of the gate metal and $\sigma(m)$ is the polarization dependent charge density.

The polynomial dependence of Fermi level (E_F) as a function of gate-source voltage (V_{GS}) proposed by Dasgupta [2.12] is used for estimating sheet carrier concentration.

$$E_F = K_1 + K_2\sqrt{n_s} + K_3 n_s \tag{2.8}$$

where K_1, K_2, and K_3 are temperature dependent parameters which are obtained for three different values of n_s and by simultaneously solving corresponding E_F equation as in [2.12]. The corresponding calculated values of K_1, K_2, and K_3 for $n_s = 2 \times 10^{14}$, 2×10^{15} and 2×10^{16} atoms per m^2 at a constant room temperature of 298 K are given in Table 2.2.

Table 2.2. Constant parameters of Fermi level model at 298 K.

Parameter	Value	Unit
K_1	-0.12562	eV
K_2	1.86342×10^{-9}	eV.m
K_3	1.0854×10^{-18}	$eV.m^2$

The values of n_s are chosen in such a way as to cover all regions of device operation i.e., from sub-threshold to strong conduction region. The polynomial approximation of the dependence of E_F and n_s makes the model simple as it is valid for all regions of device operation.

Now, substituting the E_F equation in (2.6) and solving for n_s, we obtain:

$$n_s(x) = \left[\frac{-K_2 + \sqrt{K_2^2 + 4K_4\left[V_{G1} - V(x)\right]}}{2K_4}\right]^2 \tag{2.9}$$

where: $V_{G1} = V_{GS} - V_{OFF}(m) - K_1$, $K_4 = K_3 + qd/\varepsilon(m)$, and $d = d_d + d_s$ is the total thickness of the AlGaN layer.

By using the binomial expansion formula, eqn. (2.9) can be expanded and approximated closely as (2.10),

$$n_s(x) = \alpha + \beta V(x) \tag{2.10}$$

Where:

$$\alpha = \frac{V_{G1}}{K_4} + \frac{2}{\gamma K_4}\left[1 - \sqrt{1 + \gamma V_{G1}}\right] \tag{2.11}$$

$$\beta = \frac{1}{K_4}\left[\frac{1}{\sqrt{1+\gamma V_{G1}}} - 1\right],\ \gamma = \frac{4K_4}{K_2^2} \tag{2.12}$$

2.1.2.2. Drain Current Model

The drain current can be expressed as:

$$I_D = q.n_s.W.\upsilon_D \tag{2.13}$$

where *W* is the channel width and υ_d represents the drift velocity of electrons in the channel.

The modified velocity-electric field relation has been used in the model and it can be given as,

$$\upsilon_d = \begin{cases} \dfrac{\mu E}{1+\dfrac{E}{2E_C}} & \text{for } E < 2E_C \\ \upsilon_{sat} & \text{for } E \geq 2E_C \end{cases} \tag{2.14}$$

where E is the channel electric field, μ is electron mobility, E_C is critical electric field, υ_{sat} is the electron saturation velocity, and $E_C = \upsilon_{sat}/\mu$.

Substituting (2.10) and (2.14) in (2.13) with E=dV/dx and integrating from source end of the channel (x=0) to drain end (x=L), we have

$$\int_0^L I_D.dx = Wq\mu\int_{V_1}^{V_2} n_s(x)dV - \frac{I_D}{2E_C}\int_{V_1}^{V_2} dV \tag{2.15}$$

The equivalent circuit of an AlGaN/GaN HEMT is shown in Fig. 2.2 which illustrates the upper and lower limits of integration. It is clear from the figure, the voltage at nodes V_2 and V_1 are given by $V_1 = I_D R_S$ and $V_2 = V_D - I_D R_D$, respectively.

Applying the limits and n_s approximation in (2.15), we have:

$$I_D L + \frac{I_D}{2E_C}\left[V_D - I_D(R_D + R_S)\right] = Wq\mu\int_{V_1}^{V_2}\left[\alpha + \beta V(x)\right]dV \tag{2.16}$$

Integrating the R.H.S of the above equation and solving for I_D, it leads to a quadratic equation as given below:

$$I_D^2\left[-R_D - R_S - \lambda\beta\left(R_D^2 - R_S^2\right)\right] + I_D\left[2V_L + V_D + 2\lambda\left[\alpha(R_D + R_S)\right]\right. \\ \left. + 2\lambda\beta V_D R_D\right] - \lambda V_D\left[2\alpha + \beta V_D\right] = 0 \tag{2.17}$$

where $V_L = L.E_C$ denotes the channel potential.

Eqn. (2.17) represents the generalized expression for current-voltage characteristics of extrinsic and intrinsic HEMT. The equation is of a quadratic form ($ax^2 + bx + c$) with:

$$a = -\left(R_D + R_S\right) - \lambda\beta\left(R_D^2 - R_S^2\right)$$
$$b = \left[2V_L + V_D + 2\lambda\left[\alpha\left(R_D + R_S\right) + \beta V_D R_D\right]\right] \tag{2.18}$$
$$c = -\lambda V_D\left[2\alpha + \beta V_D\right] \quad \lambda = Wq\upsilon_{sat}$$

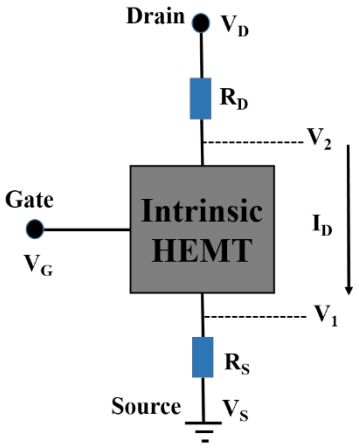


Fig. 2.2. Equivalent circuit of an extrinsic HEMT.

2.1.2.3. Intrinsic Drain Current Model

For intrinsic HEMT, substituting $R_D = R_S = 0$ in eqn. (2.17) gives the general expression for intrinsic HEMT current.

1) *Linear Region ($V_D < V_{Dsat}$):* The solution of (2.17) for I_D in linear region yields (2.19). Some of the coefficient values are negligible in (2.19) and this lead to linear variation of drain current as a function of applied drain voltage.

$$I_D = \frac{2\lambda\alpha V_D + \lambda\beta V_D^2}{2V_L + V_D} \tag{2.19}$$

2) *Saturation Region ($V_D \geq V_{Dsat}$):* For saturation region, the channel electrons saturate at a velocity defined by υ_{sat}. Then from (2.13), we have

$$I_D = q\, n_s(x)\, W\, \upsilon_{sat} \tag{2.20}$$

Also substituting $V_D = V_{Dsat}$ in (2.19) gives,

$$I_D = \frac{2\lambda\alpha V_{Dsat} + \lambda\beta V_{Dsat}^2}{2V_L + V_{Dsat}} \tag{2.21}$$

On solving (2.20) and (2.21), we obtain V_{Dsat} and I_{Dsat},

$$V_{Dsat} = \frac{2\alpha V_L}{\alpha - 2\beta V_L} \tag{2.22}$$

$$I_{Dsat} = \frac{\lambda\alpha^2}{\alpha - 2\beta V_L} \tag{2.23}$$

where V_{Dsat} and I_{Dsat} represents the voltage and current in saturation region of intrinsic HEMT operation.

2.1.2.4. Extrinsic Drain Current Model

In extrinsic HEMT, the voltage drop across the parasitic resistances is considered to be large and no longer can be neglected.

Let V_{Dmin} represents the minimum drain voltage required to saturate the HEMT in extrinsic case, considering the drop in parasitic resistances.

1) *Linear Region ($V_D < V_{Dmin}$):* The solution of (2.17) for extrinsic HEMT in linear region can be given by,

$$I_D = \frac{-b + \sqrt{b^2 - 4ac}}{2a} \tag{2.24}$$

where *a*, *b* and *c* are similar to that of the equation given in (2.18).

The solution of the above quadratic equation can be approximated accurately as,

$$I_D = \frac{-c}{b} = \frac{\lambda V_D \left[2\alpha + \beta V_D\right]}{\left[2V_L + V_D + 2\lambda\left[\alpha\left(R_D + R_S\right) + \beta V_D R_D\right]\right]} \tag{2.25}$$

2) *Saturation Region ($V_D \geq V_{Dmin}$):* The voltage required to saturate the intrinsic HEMT in extrinsic device operation is denoted by V_{Hsat} and is given by,

$$V_{Hsat} = V_{Dmin} - I_{Dsat}\left(R_D + R_S\right) \tag{2.26}$$

Substituting the value of n_s at V(x) = V_{Hsat} from (2.10) in (2.20), we have

$$I_{Dsat} = \lambda\left[\alpha + \beta V_{Hsat}\right] \tag{2.27}$$

Substituting the value of V_{Hsat} and solving for I_{Dsat} yields,

$$I_{Dsat} = \frac{\lambda\left[\alpha + \beta V_{Dmin}\right]}{\left[1 + \lambda\beta\left(R_D + R_S\right)\right]} \tag{2.28}$$

Also we know that from (2.25):

$$I_{Dsat} = \frac{\lambda V_{Dmin}\left[2\alpha + \beta V_{Dmin}\right]}{\left[2V_L + V_{Dmin} + 2\lambda\left[\alpha\left(R_D + R_S\right) + \beta V_{Dmin} R_D\right]\right]} \tag{2.29}$$

Solving for V_{Dmin} using (2.28) and (2.29), we obtain the following quadratic equation,

$$V_{Dmin}^2\left[\lambda\beta^2\left(R_D - R_S\right)\right] + V_{Dmin}\left[2\beta V_L - \alpha + 2\lambda\alpha\beta R_D\right] + 2\alpha\left[V_L + \lambda\alpha\left(R_D + R_S\right)\right] = 0 \tag{2.30}$$

The solution of quadratic equation becomes,

$$V_{Dmin} = \frac{-B + \sqrt{B^2 - 4AC}}{2A} \tag{2.31}$$

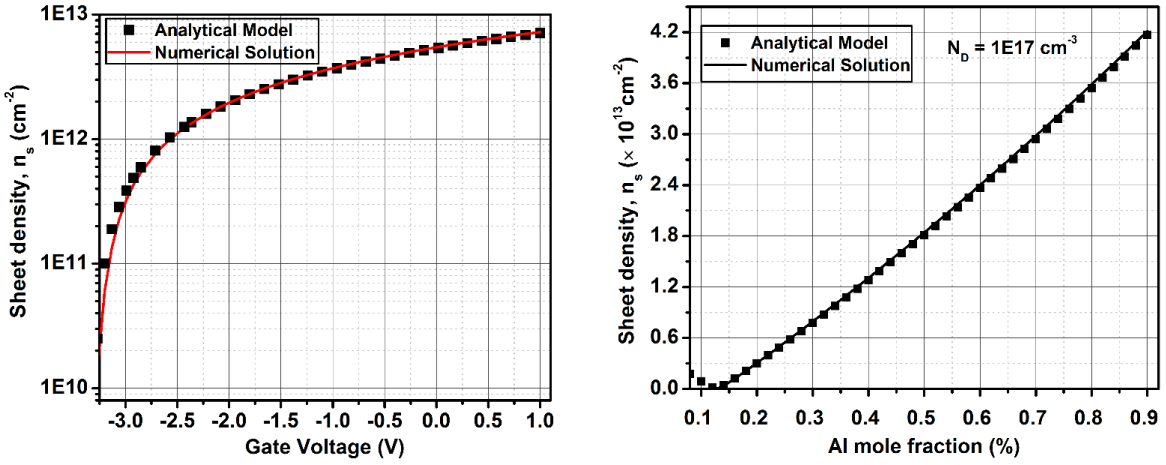
With:

$$\begin{aligned} A &= \lambda\beta^2 (R_D - R_S) \\ B &= 2\beta V_L - \alpha + 2\lambda\alpha\beta R_D \\ C &= 2\alpha\left[V_L + \lambda\alpha (R_D + R_S)\right] \end{aligned} \tag{2.32}$$

Therefore, using (2.25), (2.28) and (2.31), the extrinsic HEMT drain current characteristics can be obtained.

2.1.3. Results and Discussions

The analytically calculated sheet carrier density are compared with numerical solution result obtained by simultaneously solving (2.4) and (2.6). Fig. 2.3 (a) shows the comparison of sheet density obtained from numerical solution and analytical model, indicates a good agreement over the complete operating range of gate-source voltage. Fig. 2.3 (b) shows the comparison of sheet density obtained for various Al mole fraction using analytical model and numerical solution. A good agreement between two results demonstrates that sheet density model is valid for various Al mole fraction.

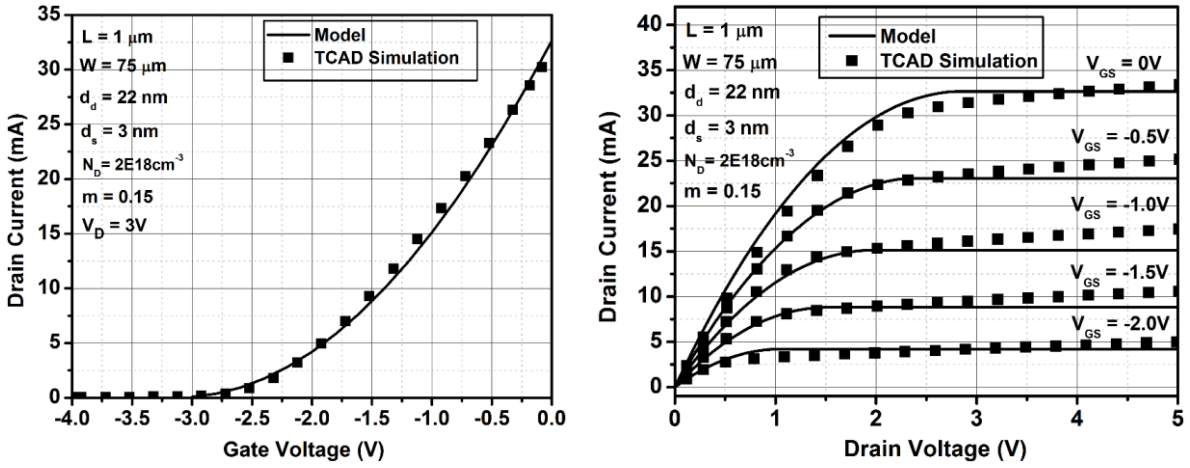


(a) (b)

Fig. 2.3. Comparison of numerical calculation and the analytical model: (a) sheet density vs. gate voltage (b) sheet density vs. Al mole fraction.

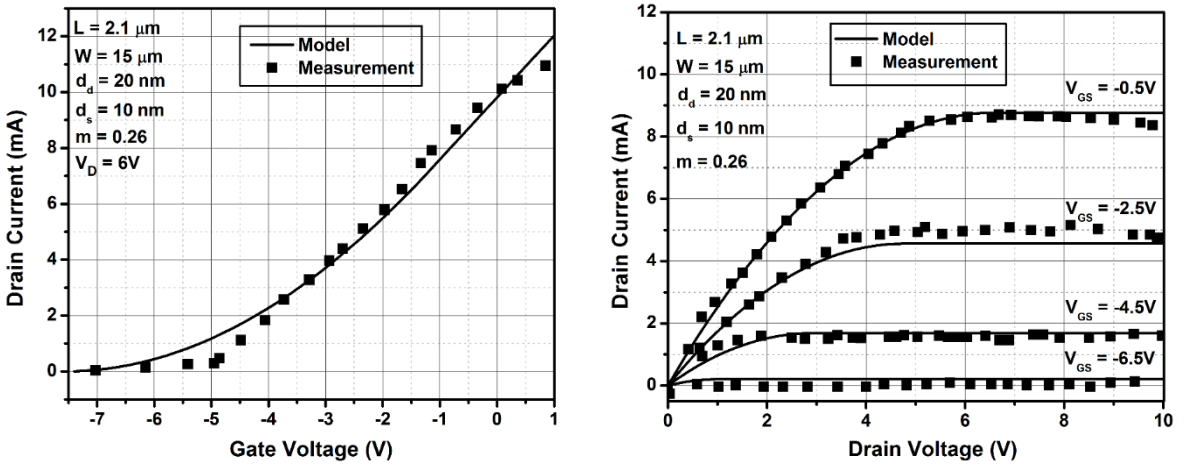
Fig. 2.4 (a) and 2.4 (b) show the comparison of I_D-V_{GS} and I_D-V_{DS} characteristics of $Al_{0.15}Ga_{0.85}N$/GaN HEMT obtained from analytical and TCAD numerical simulation results. The GaN HEMT device structure provided in [2.13] is used for TCAD simulations and analytical calculations. Poisson's and continuity equations for electrons and holes are solved

self-consistently in two-dimensional TCAD numerical simulations [2.14]. More detailed description about the methodology used in TCAD simulations are given in section 2.2. The polarization charges computed using equations described in section 2.1.2 are included at the AlGaN/GaN and AlGaN/nitride interfaces. A good agreement between the TCAD physical simulation and analytical model confirms the validity of the proposed intrinsic drain current model.



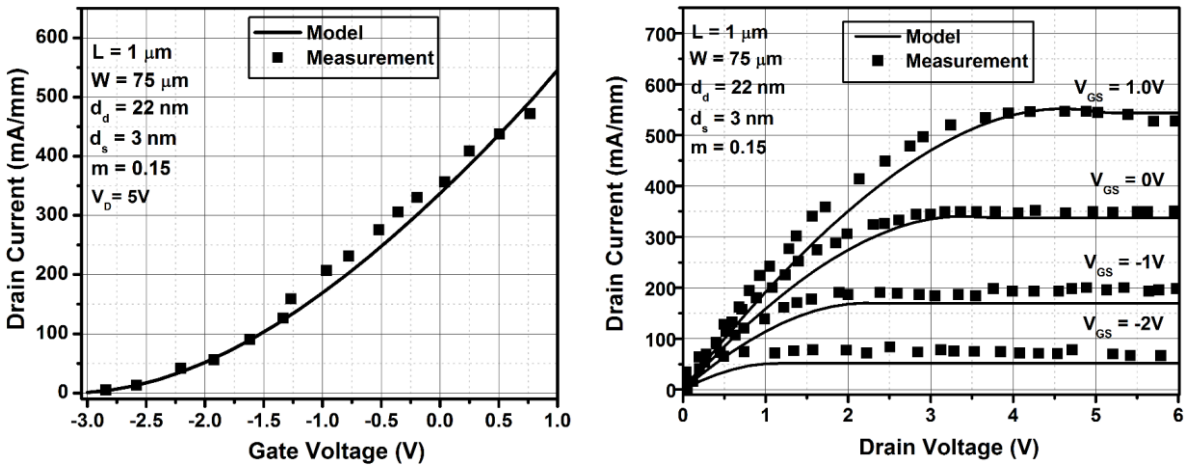
(a) (b)

Fig. 2.4. Comparison of drain current characteristics for 1-µm $Al_{0.15}Ga_{0.85}N$/GaN intrinsic HEMT calculated using analytic model (Solid lines) and TCAD physical simulation results (Points). (a) Transfer characteristics (I_D-V_{GS}) and (b) Output characteristics (I_D-V_{DS}).



(a) (b)

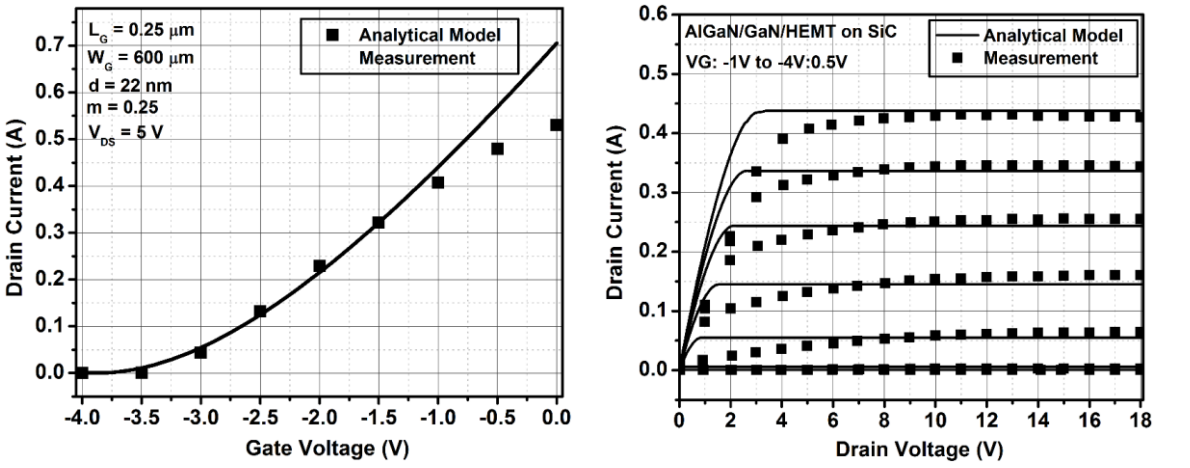
Fig. 2.5. Comparison of drain current characteristics for 2.1-µm $Al_{0.26}Ga_{0.74}N$/GaN extrinsic HEMT calculated using analytic model (Solid lines) and experimental data [2.15] (Points). (a) transfer characteristics (I_D-V_{GS}) and (b) output characteristics (I_D-V_{DS}).



(a) (b)

Fig. 2.6. Comparison of drain current characteristics for $Al_{0.15}Ga_{0.85}N$/GaN exttrinsic HEMT calculated using analytic model (Solid lines) and experimental data [2.13] (Points) for 1-µm device. (a) transfer characteristics (I_D-V_{GS}) and (b) output characteristics (I_D-V_{DS}).

Fig. 2.5 (a) shows the extrinsic I_D-V_{GS} characteristics of 2.1-µm $Al_{0.26}Ga_{0.74}N$/GaN HEMT device for the applied drain bias voltage of 6 V. Similarly, Fig. 2.5 (b) shows the I_D-V_{DS} characteristics obtained as a function of gate-source bias voltage. A good agreement is observed between the model and experimental data obtained from [2.15]. Fig. 2.6 (a) and 2.6 (b) show the comparison of I_D-V_{GS} and I_D-V_{DS} characteristics for 1-µm device obtained from our model with experimental data obtained from [2.13].



(a) (b)

Fig. 2.7. Comparison of drain current characteristics for $Al_{0.25}Ga_{0.75}N$/GaN exttrinsic HEMT calculated using analytic model (Solid lines) and in-house measured experimental characteristics (Points) for 0.25-µm device. (a) transfer characteristics (I_D-V_{GS}) and (b) output characteristics (I_D-V_{DS}).

The results of the analytical model fit reasonably with experimental data. The proposed model is valid for different dimensions such as gate width, gate lengths and AlGaN barrier layer thickness. Fig. 2.7 (a) and 2.7 (b) show the comparison of I_D-V_{GS} and I_D-V_{DS} characteristics of 0.25-µm $Al_{0.25}Ga_{0.75}N$/GaN HEMT obtained from our model and in-house measured device characteristics. In Fig 2.7 (a), the model achieves a good agreement with experimental data for higher negative gate bias and for biases close to zero, the model shows discrepancies with the measurement. Although in Fig. 2.7 (b), the model shows excellent agreement with measured characteristics in the saturation region of drain current characteristics, it shows large discrepancies in the linear region characteristics. The proposed model does not consider short channel length effect and channel length modulation phenomenon which have significant influence on submicron gate length devices. It is therefore essential to include this physical effects in the developed model to obtain a good match with experiment.

2.2. TCAD Sentaurus Simulation Methodology

The simulation tool used for the two-dimensional device simulations is Technology Computer Aided Design (TCAD) Sentaurus from Synopsys Corporation [2.16]. TCAD Sentaurus is capable of simulating a wide range of devices ranging from very deep sub-micron silicon MOSFETS to a large bipolar power transistors. In addition, it is also beneficial for simulating heterostructure devices such as SiC-MESFETs, GaN-MOSFETs and AlGaN/GaN HEMTs. It incorporates advanced physical models and robust numerical methods for simulating the electrical behavior of semiconductor devices. The main scope of the device simulations is to describe the physical process occurring inside the device structure and to understand the underlying physics behind them. This will be more helpful to enhance the performance of the new-generation devices and to improve the next-generation devices. The physical models used in the simulation are required to understand the physical mechanisms occurring in semiconductor devices. In general, the physical models available in the simulation tool are not calibrated [2.14]. Therefore, it is essential to calibrate the simulation models with the physical parameters in order to obtain the reliable prediction of the device characteristics.

In TCAD Sentaurus simulation, the real semiconductor device is represented as a virtual device (2D/3D), with physical properties that are discretized onto a non-uniform mesh of nodes. Therefore, this virtual device is an approximation of real device. The physical simulation methodology of TCAD Sentaurus is shown in Fig. 2.8. Sentaurus Device Editor (SDE) [2.17] is used to create the structure of the device, including the electrodes, doping and thermodes.

Once the device structure is created, the next step is to mesh it efficiently using Sentaurus mesh [2.18]. The device structure is divided into a number of grid points (nodes). These nodes are the points where the electrical characteristics of the device such as electric field, voltage and currents, etc. will be computed using the numerical simulations. Therefore, the meshing process has a significant influence on the device simulation. Increasing the mesh density in the simulation increases the precision of calculation, however it has a negative impact on the simulation time. It is therefore essential to make a compromise between the precision and simulation time in order to achieve the maximum benefit from physical simulation.

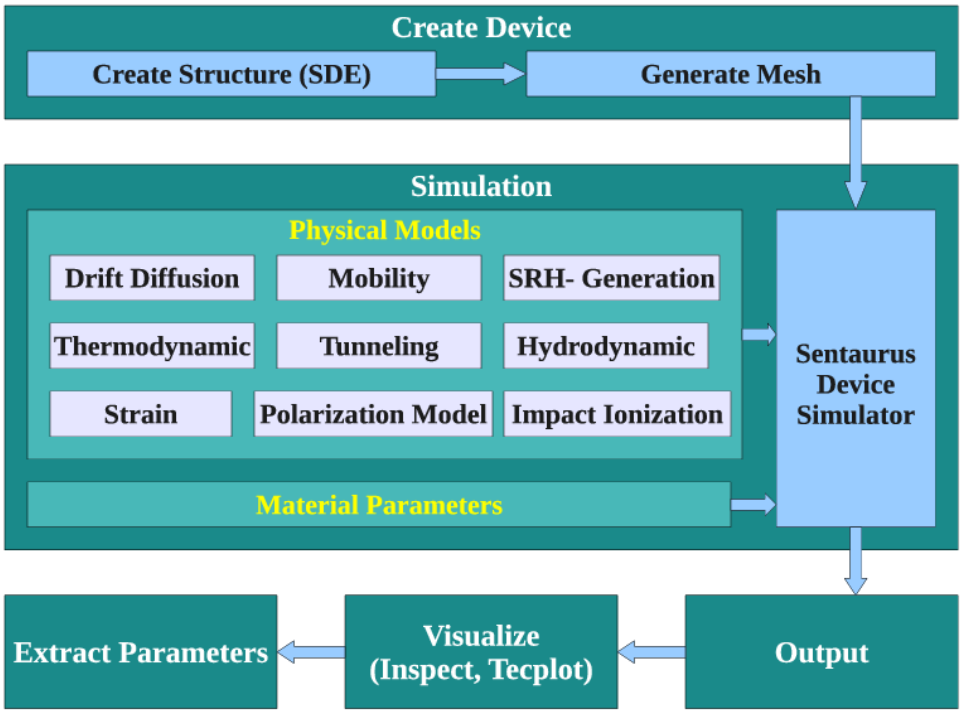


Fig. 2.8. TCAD Sentaurus physical simulation methodology.

For the case of heterostructure devices like GaN HEMT, the channel region is the AlGaN/GaN hetero-junction interface. Therefore, the mesh density must be sufficiently tight around this hetero-junction interface where the large variations in the charge carrier concentrations are observed. Sentaurus device [2.14] tool is used to define the necessary physical models required for the simulation and their associated physical material parameters. It composed of two files, a material file and the command file. The material file provides the physical parameters required for each material defined in the device structure. The command file is used to define the device contacts and the physical models to be used in the simulation. The physical models defined can

be global or for the specific region or material used in the simulation. Sentaurus device will simulate the structure and the output can be visualized using either Inspect [2.19] or Svisual [2.20] tools. Tecplot was also used in the past, however it has been replaced by Svisual for visualizing the interior of the device structure under different simulation conditions.

2.3. TCAD Physical Models

TCAD Sentaurus offers a large number of physical models to describe the physical behavior of semiconductor devices as accurately as possible to the real device. Such models need to be included in our device simulations in order to obtain some reliable predictions about the real device characteristics. In this section, the various important physical models used in the simulations are described.

2.3.1. Carrier Transport

The semiconductor equations that govern the transport of charge carriers are the Poisson's equation, which is used to solve the electrostatic potential (Ψ) self-consistently with the current continuity equations for electrons and holes and the electron and hole concentrations, n and p, respectively. The Poisson equation is given by [2.21], [2.22],

$$\nabla.\varepsilon\nabla\psi = -\rho \tag{2.33}$$

Where ε is the electrical permittivity and ρ is the charge density.

The charge density is given by [2.21],

$$\rho = q(p - n + N_D - N_A) - \rho_{trap} \tag{2.34}$$

With ρ_{trap} = q n_t for donor trap and ρ_{trap} = q (n_t -$N_{T)}$ for acceptor trap, respectively.

Where q is the electronic charge, n and p are the electron and hole densities, ρ_{trap}, n_t and N_T, N_A and N_D are the charge density contributed by traps, number of occupied traps, total number of traps, concentration of acceptors and donors, respectively.

Therefore, Poisson's equation can be written using (2.33) and (2.34),

$$\nabla.\varepsilon\nabla\psi = q(p - n + N_D - N_A) - \rho_{trap} \tag{2.35}$$

The time dependent current continuity equations for electrons and holes are given by [2.14] [2.21],

$$\frac{\partial n}{\partial t} = G_n - R_n + \frac{1}{q}\nabla.J_n \tag{2.36}$$

$$\frac{\partial p}{\partial t} = G_p - R_p + \frac{1}{q}\nabla.J_p \tag{2.37}$$

Where J_n and J_p are the electron and hole current densities, G_n and G_p are the electron and hole generation rates due to external excitation, R_n and R_p are the electron and hole recombination rates, respectively.

In a steady state condition, eqn. (2.36) and (2.37) becomes,

$$\nabla . J_n = \nabla . J_p = 0 \tag{2.38}$$

In order to achieve the self-consistent solution of Poisson's equation and the current continuity equation along with electron and hole concentrations, it is necessary to calculate the current densities, J_n and J_p from the electrostatic potential and the charge concentrations, n and p. It can be achieved by using one of the current transport models explained in the following sections.

2.3.2. Drift-Diffusion (DD) Model

The Drift-Diffusion (DD) is the TCAD Sentaurus default model which is based on approximating the semiconductor device equations in a drift-diffusion approximation to the Boltzmann transport equation (BTE). In this model, the carrier flow inside the device is due to the drift and/or diffusion under the presence of externally applied lateral or longitudinal electric field simultaneously with the generation and recombination of charge carriers. The DD model incorporated in TCAD Sentaurus numerically solves Poisson's equation and the current continuity equation self-consistently in order to obtain electron and hole concentrations, and the electrostatic potential at all the mesh nodes defined in the device structure, assuming constant temperature (carrier temperature and the lattice temperature are considered to be in equilibrium), steady state and assuming full ionization of the introduced impurities.
The current density due to the drift of carriers under the influence of applied external electric field can be given by [2.14] [2.21],

$$J_{drift} = q\left(n\mu_n + p\mu_p\right)E \tag{2.39}$$

Where E is the electric field and μ_n and μ_p are the electron and hole mobility.

When the charge carriers are distributed unevenly inside the device where they can move freely or due to the force exerted on them by an electric field, the carriers move from the region of higher gradient to the region of lower gradient. This process is called diffusion and the associated current is known as diffusion current. Diffusion current can be either in the same

direction or opposite direction of drift current. Therefore, the current density due to the diffusion of charge carriers can be given by [2.14],

$$J_{diff} = q\left(D_n \nabla n - D_p \nabla p\right) \tag{2.40}$$

Where D_n and D_p are the diffusion coefficients of electrons and holes, respectively.

In the absence of any external applied electric field, the combination of diffusion and drift current inside the semiconductor must be equal to zero.

The expression for electron concentration (n) relating the intrinsic carrier density and the intrinsic Fermi energy can be expressed as [2.14] [2.21],

$$n = n_i \exp\left(\frac{E_{F,n} - E_{Fi}}{kT}\right) \tag{2.41}$$

Where n_i is the intrinsic carrier concentration and E_i is the intrinsic Fermi energy level.
The diffusion constants, D_n and D_p defined in (2.40) are related to the electron and hole mobility in (2.39) by using Einstein's relations [2.14] [2.22]:

$$D_n = \frac{kT}{q}\mu_n \tag{2.42}$$

$$D_p = \frac{kT}{q}\mu_p \tag{2.43}$$

Under thermodynamic equilibrium conditions, the Fermi energy level for both electrons and holes are the same. However, for non-equilibrium conditions, it is not valid and therefore, quasi-Fermi levels are assumed for electrons and holes. Therefore, the relation between quasi-Fermi level, electrostatic potential and the carrier concentrations, n and p can be expressed using the following equations [2.21]:

$$\phi_n = \psi - \frac{kT}{q}\ln\left(\frac{n}{n_i}\right) \tag{2.44}$$

$$\phi_p = \psi + \frac{kT}{q}\ln\left(\frac{p}{n_i}\right) \tag{2.45}$$

Where ϕ_n and ϕ_p are the respective quasi-Fermi level for electrons and holes.
Therefore, by substituting the Einstein's relationship into the drift and diffusion current equations and using the quasi-Fermi levels definition, the total current density due to the summation of drift and diffusion current density can be given by,

$$J_n = -nq\mu_n \nabla\phi_n \tag{2.46}$$

$$J_p = -pq\mu_p \nabla\phi_p \tag{2.47}$$

2.3.3. Thermodynamic Model

The thermodynamic model (TD) is an extension of the DD model to include the self-heating effects in the device by solving the lattice heat flow equation [2.23] in addition current continuity equations and thereby estimating the impact of the temperature gradient on the current densities, assuming a single temperature for electrons, holes and the lattice of the device. This model is very useful for simulating the hetero-structure devices such as GaN HEMTs where the large amount of heat generated inside the device, due to the applied biasing conditions and therefore, analyzing the impact of this generated heat on the charge carriers is critically important. The current density equations involving the temperature gradient can be expressed as [2.14], [2.22],

$$J_n = -nq\mu_n\left(\nabla\phi_n + P_n\nabla T\right) \tag{2.48}$$

$$J_p = -pq\mu_p\left(\nabla\phi_p + P_p\nabla T\right) \tag{2.49}$$

Where T is the lattice temperature and P_n and P_p represents the thermal power generated inside the device.

2.3.4. Hydrodynamic Model

Hydrodynamic (HD) models utilize a different approach to calculate the charge carrier transport in the semiconductor devices. HD describes carrier transport based on energy balance equations to describe the non-equilibrium conditions and the energy of each type of carrier is estimated based on its own temperature conditions, and assuming a different lattice temperature [2.24]. HD model solves, self-consistently, Poisson's equation and the continuity equation along with energy balance equations for electrons, holes and the lattice.

HD model is more accurate than DD model, since DD model is incapable of reproducing the velocity overshoot effects, often observed in III-V semiconductor devices [2.25], [2.26], with sub-micron gate lengths. This is because the effect of hot electrons [2.27] is not taken into account while solving for electron and hole current densities. Moreover, it often overestimates the effect of impact ionization. Therefore, for sub-micron devices and with short gate lengths, DD model shows some discrepancies and the HD model may be more appropriate. However, the HD model is rather complex and it requires more computational effort. It often faces convergence issues and the simulation time is also often long compared to the DD model.

2.3.5. Density Gradient Method

The modern semiconductor devices such as MOSFET and GaN HEMTs have their channel lengths and oxide thickness are in quantum-mechanical scale lengths. Therefore, the wave nature of charge carriers can no longer be neglected. Moreover, in the case of AlGaN/GaN HEMT devices, the bandgap discontinuity at the hetero-junction interface forms a triangular quantum well (2DEG channel region) for the high electron mobility electrons to confine. This results in the quantization of energy levels inside the 2DEG channel. Therefore, it is essential to include the quantization model in the simulation to accurately predict the electron distribution in the channel. Unfortunately, the Schrodinger equation solver used for quantization in TCAD Sentaurus is only available for 1D simulation [2.14]. However, TCAD offers another model, density gradient method, to include the quantization effects in the simulation [2.22]. This model considers the distribution of conduction and valance band energies as discrete-like energy levels which can be used as quantization. The quantization effects are included by incorporating an additional quantization term (Λ_n) in the carrier concentration and the respective equations used in the density gradient method are expressed as [2.22]:

$$n = N_c.F_{1/2}\left(\frac{E_{F,n} - E_c - \Lambda_n}{kT_n}\right) \tag{2.50}$$

$$\Lambda_n = -\frac{\gamma h^2}{6m_n}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \tag{2.51}$$

Where Λ_n is the additional term used for the density gradient method, γ is the fitting factor, and T_n is the electron temperature and m_n is the effective mass of an electron.

The density gradient simulation is quite long compared to DD model, since it needs an additional iterative step to compute the density gradient solution.

2.3.6. Generation-Recombination Process

Generation-recombination (G-R) processes are the processes by which electron-hole pairs are created by exciting an electron from the valence band of the semiconductor material to the conduction band and thereby, creating a hole in the valence band. Both carriers eventually disappear in this process. The energy difference between the initial and final state of the electron leads to different possible classification of the recombination process. In the case of radiative recombination process, the energy is released in the form of a photon whereas for non-radiative recombination, the energy is passed on to one or more phonons. There are some standard TCAD

models available to describe the Generation-recombination process and are explained in the following section.

2.3.6.1. SRH-Recombination Model

The SRH model [2.28] describes the recombination process of electrons and holes in semiconductors occurring through the process of trapping. SRH or Trap-assisted recombination refer to the process where an electron falls into a trap, the trap gets filled and it cannot accept further electron. The electron occupying the trap moves into an empty valence band to release the captured electron thereby completing the recombination process. Therefore, this process follows two-step transition, an electron from the conduction band reaches the trap state and then to the valence band. These traps existing in the semiconductor device are due to the presence of impurities or the defects created during the crystal growth. The net recombination rate for trap-assisted recombination process is given by [2.28]:

$$R_{net}^{SRH} = \frac{np - n_{i,eff}^2}{\tau_p (n + n_1) + \tau_n (p + p_1)} \tag{2.52}$$

Using Fermi statistics, the SRH recombination rate can be modified to [2.28]:

$$R_{net}^{SRH} = \frac{np - \gamma_n \gamma_p n_{i,eff}^2}{\tau_p (n + \gamma_n n_1) + \tau_n (p + \gamma_p p_1)} \tag{2.53}$$

Where $n_{i,eff}$ is the effective intrinsic carrier concentration and τ_n and τ_p are the electron and hole lifetimes, respectively.

with,

$$\gamma_n = \frac{n}{N_C} \exp\left(\frac{E_c - E_{F,n}}{kT}\right) \tag{2.54}$$

$$\gamma_p = \frac{p}{N_V} \exp\left(\frac{E_{F,p} - E_v}{kT}\right) \tag{2.55}$$

$$n = N_C F_{1/2} \exp\left(\frac{E_{F,n} - E_c}{kT}\right) \tag{2.56}$$

$$p = N_V F_{1/2} \exp\left(\frac{E_v - E_{F,p}}{kT}\right) \tag{2.57}$$

$$n_1 = N_C F_{1/2} \exp\left(\frac{E_T - E_C}{kT}\right) \tag{2.58}$$

$$p_1 = N_V F_{1/2} \exp\left(\frac{E_V - E_T}{kT}\right) \tag{2.59}$$

Where N_C and N_V are the effective density of states for electrons and holes, $F_{1/2}$ is the Fermi-Dirac integral of order ½, E_C and E_V are the conduction and valence band energy levels, E_T is

the trap energy level and $E_{F,n}$ and $E_{F,p}$ are the quasi Fermi energy levels for electrons and holes, respectively.

2.3.6.2. Auger Recombination Model

Auger recombination is a process in which an electron and hole recombine in a band-band transition. The resulting energy arise from this process is given to another electron or hole and therefore, the involvement of third particle affects the recombination rate. The corresponding rate of band-to-band Auger recombination rate is given by [2.14]:

$$R_{net}^{A} = \left(C_n n + C_p p\right)\left(np - n_{i,eff}^2\right) \tag{2.60}$$

Where C_n and C_p are Auger coefficients.

The temperature dependent Auger coefficients can be expressed by [2.14]:

$$C_n(T) = \left(A_{A,n} + B_{A,n}\frac{T}{T_0} + C_{A,n}\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_n \exp\left(-\frac{n}{N_{0,n}}\right)\right] \tag{2.61}$$

$$C_p(T) = \left(A_{A,p} + B_{A,p}\frac{T}{T_0} + C_{A,p}\left(\frac{T}{T_0}\right)^2\right)\left[1 + H_p \exp\left(-\frac{p}{N_{0,p}}\right)\right] \tag{2.62}$$

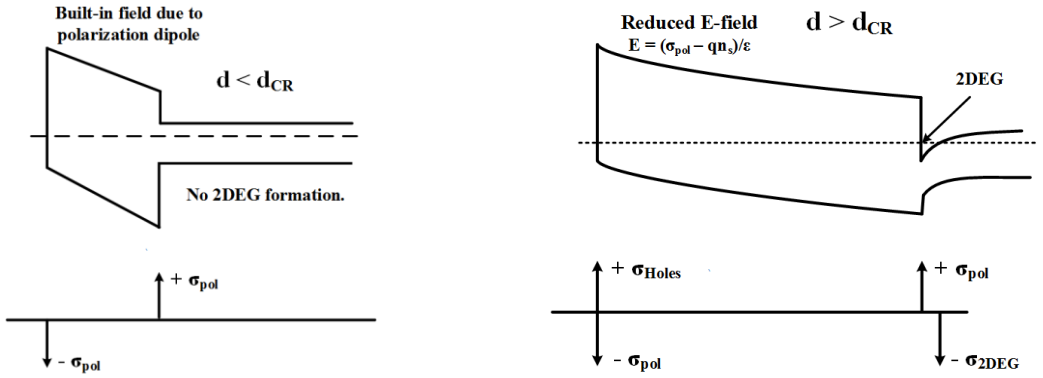
Where T_0 = 300K (room-temperature).

2.4. AlGaN/GaN HEMT Formation: Theory and TCAD Simulation Studies

2.4.1. 2DEG Formation– Ideal Surface (No surface defects)

For a conventional AlGaN HEMT device with an ideal surface, i.e. no defects and surface states are formed during the crystal growth and because of the polarization dipole existing in the AlGaN and GaN material [2.29]. The crystal grown is in equilibrium condition and hence a constant Fermi level can be assumed across the AlGaN region. The presence of this polarization dipole of same magnitude (Fig. 2.9 (a)) is not sufficient to induce the 2DEG at the AlGaN/GaN interface. When the thickness of the AlGaN region (d) is increased, the valence band of AlGaN barrier approaches the Fermi level at the surface (Fig. 2.9 (b)). This facilitates the transfer of electrons from the valence band of AlGaN barrier to the conduction band of GaN, causing the accumulation of holes at the surface. Therefore, a positive sheet charge is formed at the surface and an equivalent negative sheet charge (2DEG) is formed at the AlGaN/GaN interface. Note that no 2DEG is formed until the surface hole gas is created. Moreover, the formation of surface hole gas strongly depends on the thickness of the AlGaN region. The minimum AlGaN

thickness needed to induce the surface hole gas or 2DEG is referred to as the critical thickness (d_{CR}) [2.29]. Furthermore, this value of critical thickness depends on the bandgap of the AlGaN material and also on the magnitude of polarization dipole induced in the crystal structure.



(a) (b)

Fig. 2.9. 2DEG Formation for the case of an ideal surface: (a) No 2DEG ($d < d_{CR}$) (b) 2DEG is formed at the AlGaN/GaN interface ($d > d_{CR}$) [2.29].

2.4.2. 2DEG Formation–Surface Donors

In case of a non-ideal surface i.e. the surface of the AlGaN region is expected to contain certain vacancies or other defects. The surface states thus formed constitute a net positive charge as shown in Fig. 2.10 [2.30]. The energy level of this surface state is presumed to be constant during the growth of AlGaN region. It is also important to note that the Fermi level remains constant as the crystal is under equilibrium condition. The schematic of the conduction band diagram for a conventional AlGaN/GaN HEMT structure with its associated space charge component is shown in Fig. 2.10. In the absence of any external electric-field, the sum of the various space charges induced is zero, in order to maintain the overall charge neutrality of the device [2.30]. Moreover, the polarization dipoles ($\pm \sigma_{pol}$) induced are of equal magnitude and opposite in sign and thus the net contribution of total polarization charges is exactly zero. The modulation doping in the AlGaN barrier ionizes some of the dopants (σ_{AlGaN}) and contributes to the formation of 2DEG (n_s). Therefore, the charge balance equation under equilibrium conditions can be expressed by [2.30]:

$$\sigma_{surface} + \sigma_{AlGaN} - q.n_s = 0 \qquad (2.63)$$

Equation 2.63 states that the total number of electrons in the 2DEG region can be given by the sum of ionized dopants in the AlGaN barrier and the ionized surface donors ($\sigma_{surface}$).

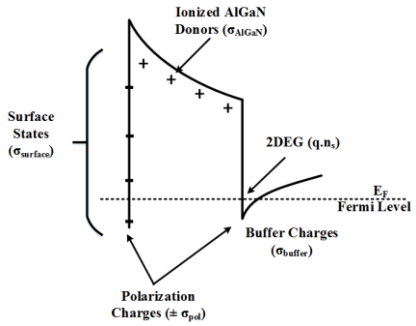
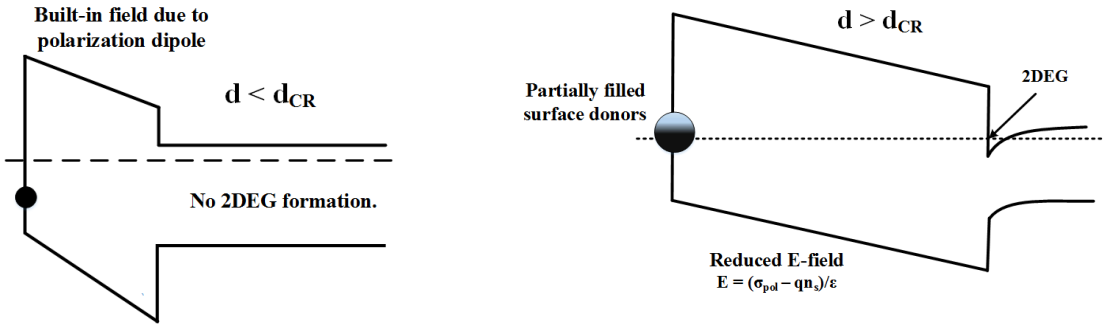


Fig. 2.10. Band diagram of a conventional AlGaN/GaN HEMT illustrating various space charges [2.30].

However, for the case of an un-doped HEMT structure, the 2DEG formed at the hetero-junction interface is only because of the surface donors. The surface donors with the energy E_D are ideally located below the conduction band (Fig. 2.11 (a)). Moreover, these donor-like states are neutral when occupied and positive when they are empty. If the surface donors are sufficiently deep inside the conduction band i.e. the E_D lies well below the Fermi level E_F, no 2DEG formation occurs at the hetero-junction interface. However, there is a constant electric field in the AlGaN barrier owing to the polarization charges.



(a) (b)

Fig. 2.11. 2DEG Formation with surface donors [2.30]: (a) No 2DEG ($d < d_{CR}$) (b) 2DEG is formed at the AlGaN/GaN hetero-junction ($d > d_{CR}$).

As the AlGaN region thickness increases, $E_F - E_D$ decreases and at the critical AlGaN thickness d_{CR}, the surface donor energy level reaches the Fermi level (Fig. 2.11 (b)). Electrons are then able to transfer from the surface donors to the AlGaN/GaN hetero-junction interface and leaves a positive charges at the surface. This theory of surface states as the origin of 2DEG at the hetero-junction interface of an un-doped AlGaN/GaN HEMTs was first proposed by Ibbetson [2.30]. The solution of Poisson's equation for the critical AlGaN barrier thickness (d_{CR}) to form the 2DEG density can be given by [2.30]:

$$d_{CR} = \frac{\varepsilon\left(E_D - \Delta E_C\right)}{q.\sigma_{pol}} \tag{2.64}$$

where ε is the dielectric constant of the AlGaN and ΔE_C is the conduction band offset between AlGaN and the GaN material.

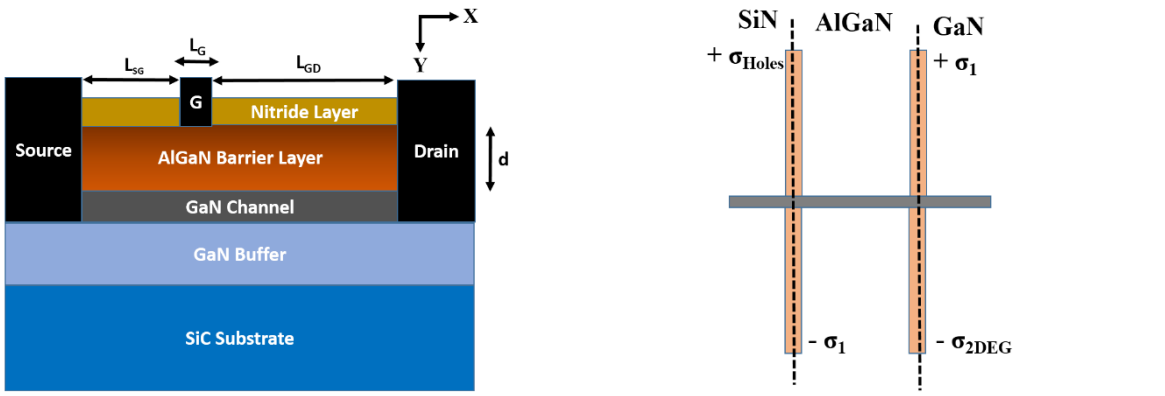
The 2DEG density as a function of AlGaN barrier thickness for $d > d_{CR}$ can be given by [2.30]:

$$q.n_s = \frac{\sigma_{pol}\left(1 - d_{CR}\right)}{d} \tag{2.65}$$

The 2DEG sheet density increases rapidly for $d > d_{CR}$ and with further increase in AlGaN barrier thickness ($d \gg d_{CR}$), the 2DEG density gradually approaches σ_{pol}/q, since the electric field in the AlGaN barrier approaches zero for $d \gg d_{CR}$ [2.30]. In other words, as the thickness of AlGaN barrier thickness increases ($d > d_{CR}$), all the electrons from the surface states have already moved to the AlGaN/GaN hetero-junction interface and at a certain value of d_{CR}, the 2DEG density saturates approximately equals to surface trap density.

2.4.3. TCAD Simulation: 2DEG Formation – Ideal Surface

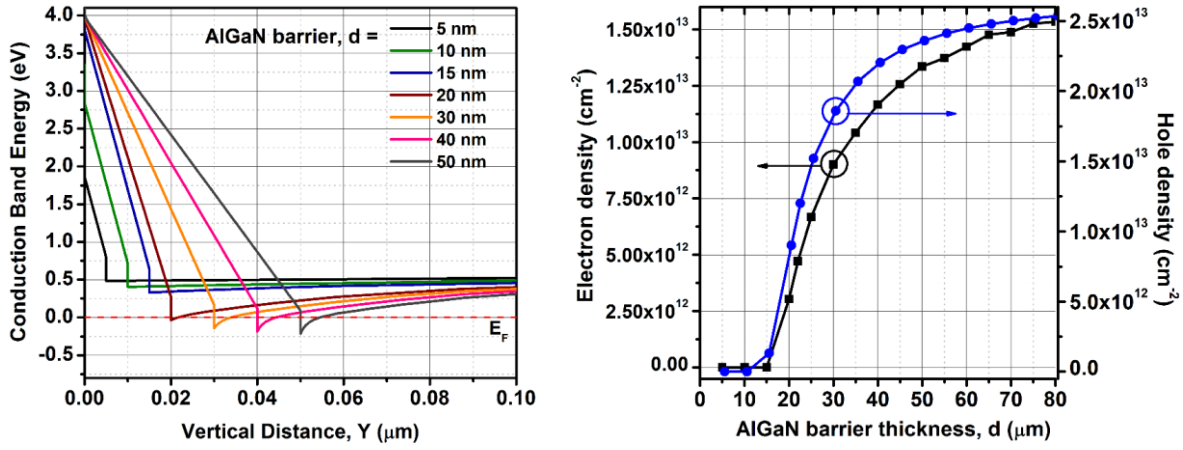
In order to understand the principle of formation of the 2DEG in an AlGaN/GaN HEMT heterostructure, two-dimensional (2D) TCAD physical simulations have been performed. The conventional AlGaN/GaN structure used in the simulation are shown in Fig. 2.12 (a). The gate length (L_G) and width (W_G) of the device are 0.25 and 600 µm, respectively. The polarization charges defined in the physical simulator at each material interface is shown in Fig. 2.12 (b). The Al mole fraction (m) of the AlGaN material is assumed to be 20%. The value of σ_1 is set to 1.1×10^{13} cm^{-2}. This has been calculated based on the theoretical procedure given in [2.6].



(a) (b)

Fig. 2.12. (a) Cross section of the conventional AlGaN/GaN HEMT structure. (b) Polarization charges defined in the physical simulation.

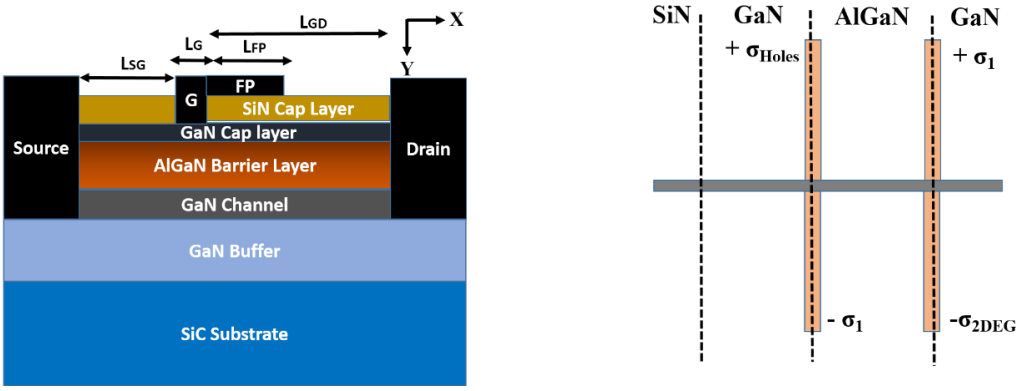
The simulated conduction band diagram as a function of AlGaN barrier thickness is shown in Fig. 2.13 (a). For barrier thicknesses less than 20 nm, no channel formation occurs. The corresponding electron and hole density as a function of AlGaN barrier thickness (d) under zero-bias conditions is shown in Fig. 2.13 (b). It is clear that when the AlGaN barrier thickness is less than critical thickness (d_{CR} =20 nm), the surface hole density is close to zero and hence, there is no 2DEG formed in the channel region. However, the increase in AlGaN barrier thickness after the critical thickness ($d > d_{CR}$) causes the linear increase in 2DEG density and eventually it saturates for larger AlGaN barrier thickness ($d \gg d_{CR}$). This confirms that for the ideal surface HEMT structure, the 2DEG density formed at the AlGaN/GaN hetero-junction interface is due to the accumulation of holes at the surface.



(a) (b)

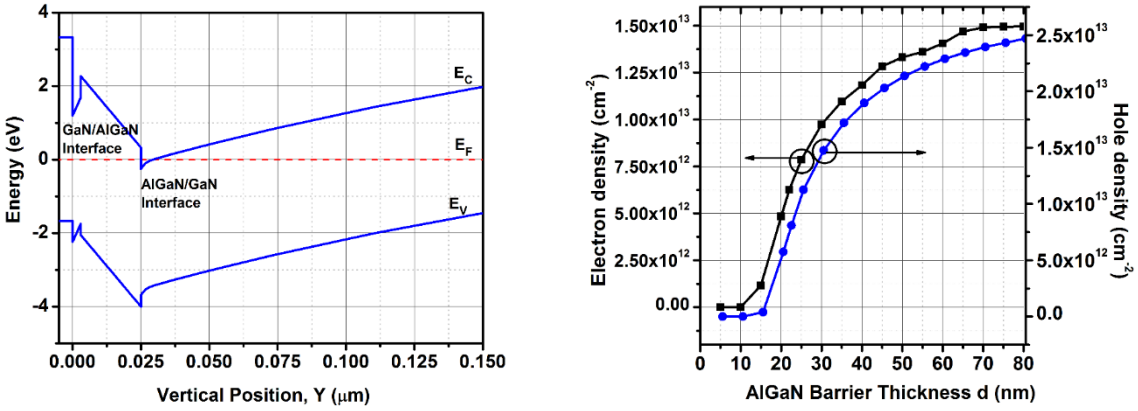
Fig. 2.13. (a) Simulated conduction band diagram and (b) electron and hole density as a function of AlGaN barrier thickness (d) under zero-bias conditions. Critical AlGaN barrier thickness, d_{CR} = ~20nm.

In order to validate the aforementioned hypothesis, another TCAD simulation study has been performed by including a few-nm GaN cap layer. The schematic cross section of the device structure and the polarization charges defined in the physical simulation are shown in Fig. 2.14 (a) and (b), respectively. The thickness of the GaN buffer along with the GaN channel region is 1.7-µm. The simulated energy band diagram under zero-bias conditions and for AlGaN barrier thickness of 22 nm is shown in Fig. 2.15 (a). The simulated electron and hole density as a function of AlGaN barrier thickness are shown in Fig. 2.15 (b). The electron and hole density increases linearly and then saturates with AlGaN barrier thickness. It is important to note that the surface holes are accumulated at the GaN-cap and AlGaN barrier interface where the negative polarization charges are defined.



(a) (b)

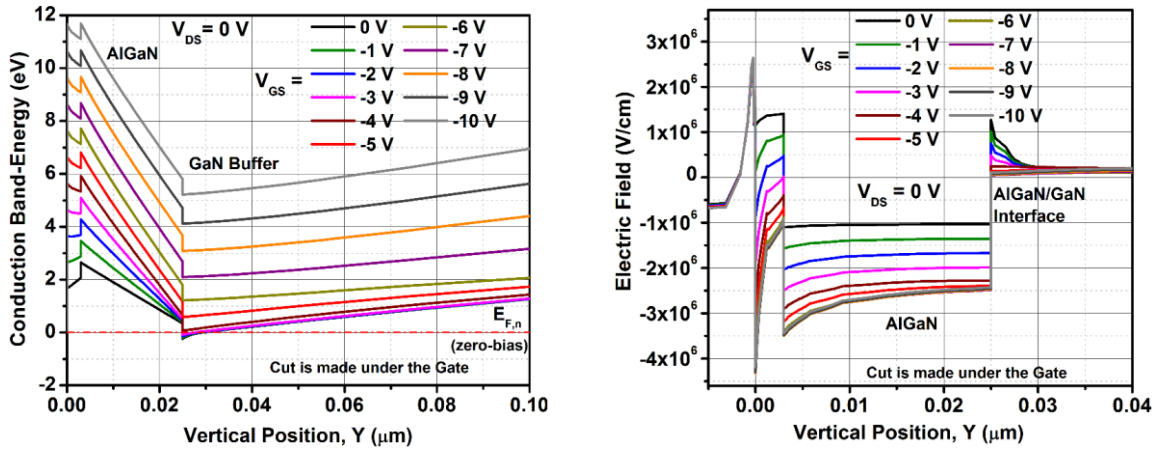
Fig. 2.14. (a) Schematic cross section of the GaN/AlGaN/GaN HEMT structure. (b) Polarization charges defined in the TCAD simulation.



(a) (b)

Fig. 2.15. Zero-bias conditions: (a) Simulated energy band diagram. Conduction band is shifted above the Fermi level due to iron (p-type) doping in the GaN buffer. (b) Electron (2DEG) and hole density of GaN/AlGaN/GaN HEMT as a function of AlGaN barrier thickness (*d*). Critical AlGaN barrier thickness, d_{CR} = ~20nm, Al mole in AlGaN barrier = 20%.

The corresponding 2DEG is formed at the AlGaN barrier and GaN channel interface. Fig. 2.16 (a) shows the simulated conduction band energy of the structure under different gate-bias conditions (V_{GS}) and at drain bias, V_{DS} =0V. The pinch-off voltage of the simulated device is around -3.5 V. It can be seen from the Fig. 2.16 (a) that for gate-bias voltage between 0 and -4V, the 2DEG quantum well formed at the AlGaN/GaN hetero-junction interface is clearly visible and for higher gate-biases, the quantum well disappears and hence, there are no electrons confined at the hetero-interface. The simulated electric field along the cross section of the device and for different gate-bias conditions and at drain bias, V_{DS} =0V is shown in Fig. 2.16 (b). The electric field along the AlGaN/GaN interface decreases as the gate bias increases, due to the depletion of electrons in the channel region.



(a) (b)

Fig. 2.16. Simulated conduction band diagram (a) and electric field along the vertical cross section of the structure (b) under different gate-biases and at V_{DS} =0V.

2.4.4. TCAD Simulation: 2DEG Formation –Surface Donors

The TCAD simulations have been performed by including the donor-like traps at the surface by using the same structure as shown in Fig. 2.14 (a). The polarization charges defined in the simulation is shown in Fig. 2.17 (a). The polarization charges for various Al mole fraction (*m*) has been calculated based on Ambacher [2.6] method and are used in the simulations. The value of σ_1 is calculated as 1.0× 10^{13} cm^{-2}. The magnitude of interface charges defined at the Nitride/GaN cap interface, σ_2 is -2.0× 10^{12} cm^{-2}. Donor-like traps are introduced at the surface of the device with a concentration (N_{TD}) of 1.0× 10^{13} cm^{-2} and energy level of 0.2 eV below the conduction band.

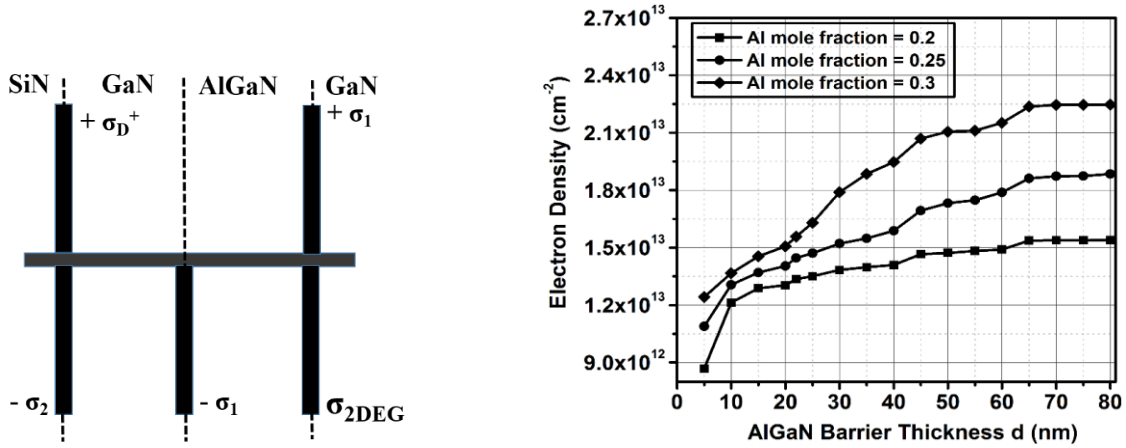
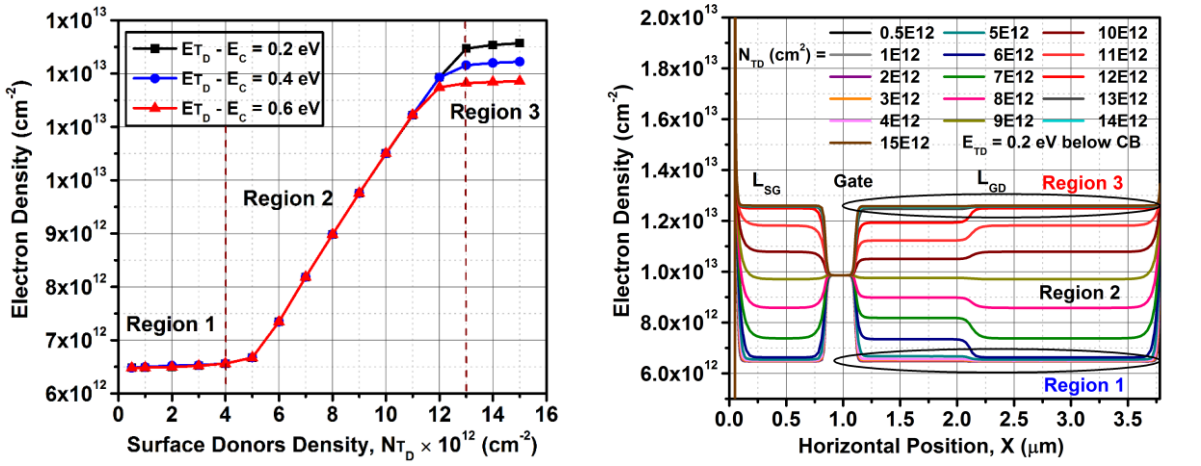


Fig. 2.17. (a) Polarization charges defined in the physical simulation (b) Simulated electron (2DEG) as a function of AlGaN barrier thickness (*d*) and for various *m*, under zero-bias conditions.

The simulated electron density for various Al mole fraction and AlGaN barrier thickness (*d*) is shown in Fig. 2.17 (b). The 2DEG density increases linearly with AlGaN barrier thickness and then saturates for each Al mole fraction. The magnitude of electron density increases with the increase in Al mole fraction.

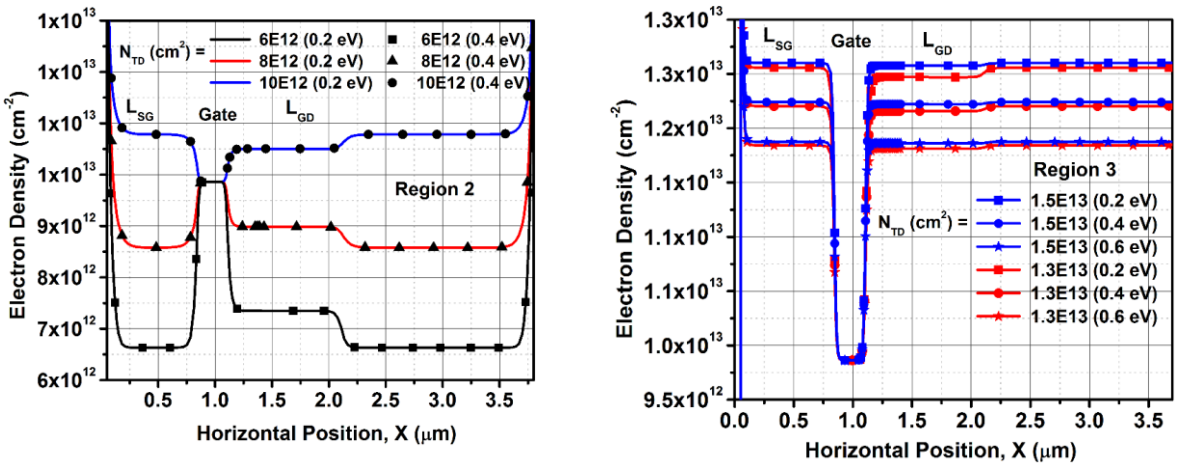
2.4.5. Surface Donors– Influence of donor density and energy level

The influence of surface donor density (N_{TD}) and energy level (E_{TD}) on the 2DEG sheet density under zero-bias conditions have been studied [2.31]. Fig. 2.18 (a) shows the variation of 2DEG density in the channel region as a function of surface donor's concentration, three regions have been identified [2.31] as the surface donors density varies from 1.0× 10^{12} to 1.6× 10^{13} cm^{-2}, respectively. Fig. 2.18 (b) shows the variation of 2DEG density as a function of device distance (horizontal cut) for various donor density and energy level values. In Region 1, the surface donor density is too low and hence it does not show much influence on the simulated 2DEG density. In Region 2, the 2DEG density increases linearly with the assumed donor density and is independent of the defined trap energy level, E_{TD} (Fig. 2.19 (a)). However, in Region 3, the 2DEG density becomes independent of the donor density but the location of trap energy level with respect to conduction band strongly influences the 2DEG density (Fig. 2.19 (b)). The threshold value that defines the boundary between regions 1 and 2 could be determined based on the magnitude of the interface charges defined at the Nitride/GaN-cap interface [2.31].



(a) (b)

Fig. 2.18. (a) Simulated 2DEG density as a function of surface donor density. Three regions can be clearly visible as the surface donor density is varied (N_{TD}). (b) Simulated 2DEG density as a function of horizontal device distance (X) for various surface donors density and for E_{TD} = 0.2 eV under zero-bias (equilibrium) conditions.



(a) (b)

Fig. 2.19. Simulated 2DEG density as a function of horizontal device distance (X) for various surface donors density and energy levels under zero-bias (equilibrium) conditions: (a) Region 2 and (b) Region 3.

The increase in the donor density compensates the negative interface charge and the further increases in donor density in Region 2 contribute electrons to the channel. Moreover, the introduced donor traps are ionized and hence the electric field in the barrier region decreases with the increase in 2DEG density in the channel region. However, this electric field is sufficiently high in this region to bring down the conduction band minimum at the surface and therefore, the trap energy level, E_{TD} lies well above the Fermi energy level (Fig. 2.20) to ionize the surface donor traps.

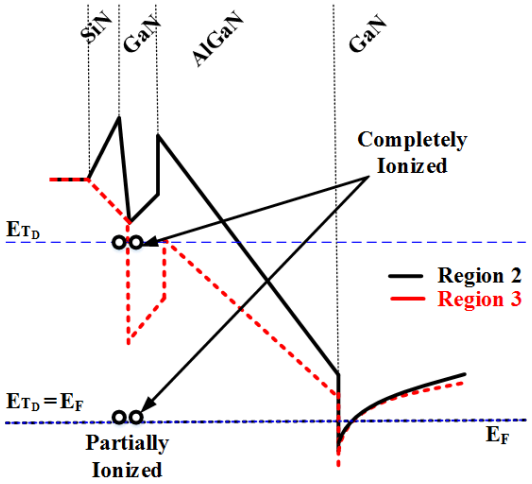
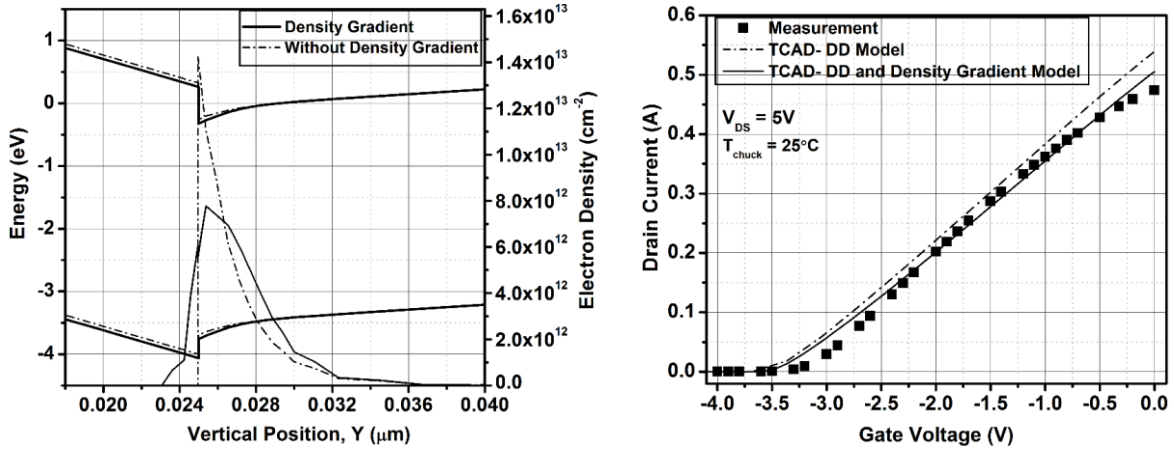


Fig. 2.20. Schematic of the conduction band diagram illustrating the influence of donors on the 2DEG density in Regions 2 and 3. If the trap energy level (E_{TD}) lies well above E_F, all donor traps are completely ionized and if $E_{TD} = E_F$, traps are partially ionized [2.31].

Furthermore, in this region (Region 2), the donor trap density is not sufficient to pin the Fermi energy level (E_F) at the donor trap energy level. In the Region 3, the magnitude of the introduced donor density is higher and this causes the reduction of electric field in the AlGaN barrier region and eventually the trap energy level approaches the Fermi energy level (Fig. 2.20). The region where the trap energy level equals the Fermi energy level is the Fermi-level pinned region. It can be visualized in Fig. 2.18, where the 2DEG density saturates (Region 3). Therefore, any further increase in donor density will result in the ionization of very few donors and the 2DEG density remains unchanged. However, if the trap energy level is varied, it will alter the distance of the trap energy level from the Fermi energy level and this will influence the ionization of donor traps in this region [2.31]. For instance, if the energy difference between the conduction band and the trap level is increased, the 2DEG sheet density saturates for lower values of surface donors, since E_{TD} lies closer to E_F and hence only few ionized donors are sufficient enough for pinning E_F.

2.5. Comparison of Density-Gradient and Drift-Diffusion Simulation

Fig. 2.21 (a) shows the simulated electron density and energy band diagram along the vertical cross section of the GaN HEMT structure shown in Fig. 2.14 (a) at zero-bias conditions and with and without invoking the density gradient model. It is evident from the electron density plot that the density gradient simulation more accurately reproduces the electron distribution by considering the wave-like nature behavior of the electrons confined in the 2DEG quantum well. Moreover, it is important to note that the peak electron concentration is located slightly away from the hetero-junction interface in the density gradient simulation, due to the wave mechanics associated with the insignificant penetration of the electron wave function into the AlGaN barrier. Fig. 2.21 (b) shows the comparison of the measured and simulated transfer characteristics of the device. The density gradient simulation shows slight reduction in drain current because of the quantum potential corrections applied to the current continuity equation. However, for deep class AB operation mode (I_D <100mA), the density gradient and classical simulation approach yields an approximately similar result. Moreover, the density gradient approach takes more simulation time and therefore, classical drift-diffusion simulation approach is used for all the simulations reported here.



(a) (b)

Fig. 2.21. Simulated energy band diagram and electron density in the channel (a) and transfer characteristics of the 8×75 µm GaN HEMT device (b), with and without invoking the density gradient quantization model.

2.6. Comparison of Drift-Diffusion and Hydrodynamic Simulation

It has been well established that drift-diffusion simulation is often inaccurate for simulating the sub-micron gate length devices. Fig. 2.22 shows the comparison of the simulated output characteristics of the 8×75 µm AlGaN/GaN HEMT device (with L_G = 0.25 µm), using the drift-diffusion and hydrodynamic simulation methods. It is evident at higher gate biases, there is some discrepancy observed between the DD and hydrodynamic model. The higher gate biases, results in increasing electric fields under the gate region, causing the underestimation of the drain current by the DD model. However, for lower gate biases, the results are nearly identical.

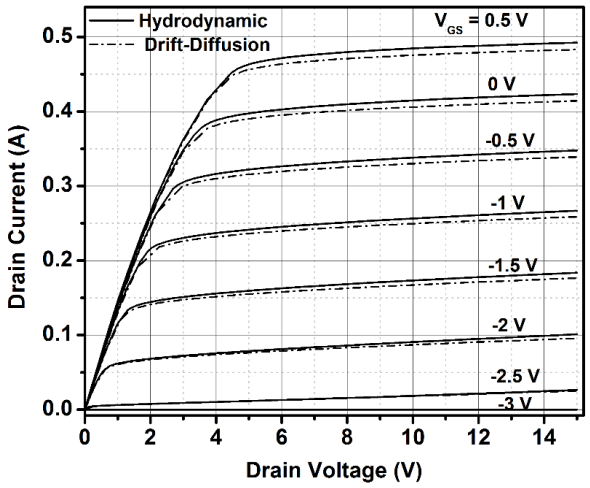


Fig. 2.22. Comparison of the simulated output characteristics of the 8×75 µm GaN HEMT device using the drift-diffusion and hydrodynamic simulation approach.

Fig 2.23 shows the simulated electron temperature inside the device for different drain bias conditions. The hydrodynamic model is more useful to study the variation of charge carrier temperature (electrons and holes) inside the device. It is evident from Fig. 2.23, at higher drain biases, the hot spot is clearly visible at the drain-side edge of the gate terminal and in the gate-drain region. The hydrodynamic simulation gives more accurate results, however the simulation time is very high and often faces the convergence issues. In this thesis, all the measurements are performed under deep class-AB operation mode, therefore, drift-diffusion simulation model is sufficient for all our analysis.

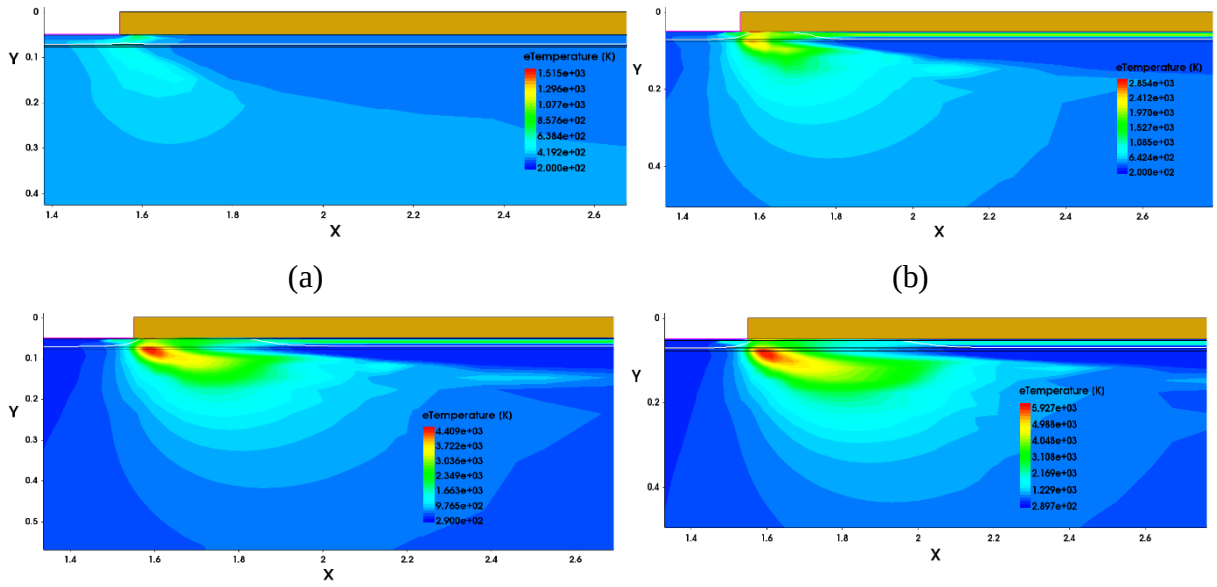


Fig. 2.23. Simulated electron temperature inside the device at V_{GS} = 0.5 V and V_{DS} = 5 V (a), 10 V (b), 15 V (c) and 20 V (d). Hot spot is visible in the drain-side of gate edge at higher drain biasing conditions.

2.7. Summary

In the first section of this chapter, a simple analytical model of current-voltage characteristics of AlGaN/GaN HEMT, valid for both intrinsic and extrinsic HEMT has been presented. The proposed model accounts for the effect of polarization charge density in estimating the 2DEG sheet carrier density, pinch-off voltage and also determining the current-voltage characteristics of AlGaN/GaN HEMT. The influence of Al mole fraction and AlGaN barrier layer thickness have been considered in the developed model. The effect of source and drain resistances have also been incorporated to accurately predict the extrinsic HEMT device characteristics. The proposed model does not include some physical effects like channel length modulation, short

channel effect, mobility degradation and self-heating. However, the proposed model achieves a reasonable agreement with experimental results for long channel devices. As a future extension to this work, all the aforementioned physical effects will be incorporated into the model to accurately predict the device characteristics.

The second section of this chapter provides an overview of the TCAD Sentaurus simulation software from Synopsys Corporation. The simulation methodology implemented by the TCAD Sentaurus has been described in detail. The basic semiconductor expressions such as Poisson's equation, drift and diffusion current and current continuity equations for electrons and holes are provided. Further, the three different kind of simulation methods, drift-diffusion, thermodynamic and hydrodynamic have been explained. The basic theory behind the formation of the 2DEG in AlGaN/GaN heterostructure has been explained using theoretical diagrams. TCAD simulations results which illustrate the principle of 2DEG formation have been provided. The quantum correction using a density-gradient simulation method has been described in detail. The comparison of drift-diffusion and hydrodynamic simulation results of AlGaN/GaN HEMT devices demonstrate that, for lower gate-biases, both the DD and HD models achieve approximately the same results. Therefore, this suggests that the DD model is sufficient to analyze the deep class-AB operation mode device characteristics, which will be discussed in chapters 3 and 4.

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Chapter 3

GaN/AlGaN/GaN HEMTs on SiC Substrate: Investigation of Trapping Mechanisms through Measurements and TCAD Physical Simulations

Based on Publications:

1. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby, Raphael Sommet and Raymond Quéré, "Identification of GaN Buffer Traps in Microwave Power of AlGaN/GaN HEMTs through Low Frequency S-Parameters Measurements and TCAD-Based Physical Device Simulations", *IEEE Journal of the Electron Devices Society*, vol. 5, pp: 175 – 181, May 2017.

2. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby, Michel Prigent and Raymond Quéré, " Low Frequency Noise Characterization in GaN HEMTs: Investigation of deep levels and their physical properties", *IEEE Electron Device Letters*, vol. 38, pp: 1109 – 1112, Aug. 2017.

3. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby and Raymond Quéré, "Low Frequency Drain Noise Characterization and TCAD Physical Device Simulations: Identification and analysis of GaN buffer traps", *IEEE Electron Device Letters*, in press, Nov. 2017.

4. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby and Raymond Quéré, "Drain-Lag Characterization and TCAD-based Device Simulations of GaN HEMTs: Identification of physical location of traps causing drain-lag effects", *IEEE Trans. on Electron Devices*, in preparation, Oct. 2017.

Chapter 3. GaN/AlGaN/GaN HEMTs on SiC Substrate: Investigation of Trapping Mechanisms through Measurements and TCAD Physical Simulations

3.1. Introduction

In recent years, GaN material has received significant attention due to its superior material properties such as wide bandgap, high electron mobility, high saturation velocity and high breakdown electric field [3.1], [3.2]. Moreover, there has been tremendous development focused on the growth of GaN high electron mobility transistor (HEMT) device technology including improving the material quality of epitaxial [3.3] and passivation layers [3.2], selecting the appropriate substrate materials [3.3], [3.4] implementing the field plates [3.2] [3.5] and ultra-short gate lengths [3.6], [3.7] and optimizing the AlGaN barrier thickness [3.6]. Also, in order to eliminate short-channel effects in nano-scale devices, it is necessary to render the GaN buffer semi-insulating by either using intrinsic defects or extrinsic deep-level dopants such as iron (Fe) or Carbon (C) [3.8] [3.9]. These deep level dopants are used to confine the charge carriers in the channel [3.9] and also they suppress buffer leakage, punch-through and other short-channel effects [3.9]. All these technological improvements have enabled GaN HEMT technology to act as a disruptive technology for high-power microwave and mm-wave applications [3.10]. Therefore, GaN HEMT device is capable of delivering high breakdown voltage, high switching speed and low on-resistance (R_{ON}), which makes it ideal for power switching applications [3.11].

Although GaN HEMT devices have demonstrated their superior performance [3.3], [3.6], the presence of deep levels in the structure degrades the dynamic device performance [3.12]. Indeed, the density of two-dimensional electron gas (2DEG) at the heterostructure interface is altered due to the capture of electrons by the deep traps either present at the surface, or barrier or buffer layer [3.12] . Moreover, these traps are slow in nature and thus undermine the device reliability [3.13], [3.14]. Several types of trapping effects have been reported in the literature [3.11]–[3.13]. However, the origin and properties of these traps remain unclear. Trapping effects cause current collapse – a recoverable reduction in drain current after the application of high biasing voltage, transconductance-frequency dispersion, gate lag, drain lag, and restricted microwave output power [3.11]. Several studies have also demonstrated that the presence of an Fe-doped GaN buffer causes an enhancement in the current collapse mechanism [3.15] and thereby the device deviates from expected microwave performance. Therefore, the analysis of traps and identifying the ways to minimize the influence of trapping effects on device

performance is an active research area. There are various measurement techniques [3.11]–[3.18], such as deep level transient spectroscopy (DLTS), gate and drain lag transients, high-voltage transient CV, frequency dependent transconductance dispersion and low frequency noise (LFN) measurements are available to investigate the trapping behavior of the GaN HEMT devices.

This chapter investigates the trapping effects in the GaN HEMT devices using low frequency measurements and TCAD-based physical device simulations. The chapter is divided into three sections. In the first section, we describe the experimental methodology used for characterizing the GaN buffer traps and also discusses the extraction of trap parameters from LF S-parameters measurements. Furthermore, we also present the TCAD physics based simulation results to validate our measurement technique. In the second section, characterization of GaN buffer traps using LF noise measurements and simulation studies have been explained. In the final section, we attempt to investigate the influence of trapping effects such as gate and drain-lag on the simulated I-V characteristics using transient simulations.

3.2. Traps

Traps are generally created due to material defects, dislocations formed during the crystal growth, lattice mismatch between two materials, the difference in thermal expansion coefficients between substrate and the epilayers, the presence of impurities in the crystal lattice and the existence of dangling bonds on the surface of the crystal structure [3.19]–[3.21]. These defects and dislocations can acts as the potential charge carrier traps and creates a localized trap levels inside the bandgap of the material. The majority of the trapping mechanisms would result in similar effect of degradation on the device characteristics, especially at high frequencies. However, the characteristics time of the emission process in GaN HEMTs can range from a few nanoseconds to several seconds [3.21]. As a consequence, the trapping mechanisms could limit the device performance even at low frequencies. Moreover, these trapping effects could contribute significantly to the low-frequency noise [3.21]. It is also important to note that the different fabrication process technique results in inducing various trapping centers. Therefore, it is essential to understand the phenomenology of these traps, their physical location and the mechanisms involved, in order to optimize the future performance of GaN HEMT device technology.

Traps can be classified into two types: donor-like and acceptor-like traps. A donor-like traps is considered to be positive if empty and neutral if filled with an electron, whereas an acceptor-like traps is neutral if empty and negative, if occupied. A trap can be defined by its energy level inside the bandgap, which is associated with the following parameters:

The probability of trap occupation under equilibrium conditions is given by the Fermi function [3.23]:

$$f_{t,eq} = \frac{1}{1 + e\left(\frac{E_T - E_{Fo}}{kT}\right)} \tag{3.1}$$

Similarly, the probability of trap occupation under non-equilibrium conditions can be given using the quasi-trap Fermi level [3.23]:

$$f_{t,non-eq} = \frac{1}{1 + e\left(\frac{E_T - E_{FT(x,y,z)}}{kT}\right)} \tag{3.2}$$

Where E_F is the Fermi energy level, k is the Boltzmann constant (eVT^{-1}) and T is the temperature (K).

The trap can be defined by using the electron (σ_n) and hole (σ_p) cross section parameters, respectively. The relationship between the trap cross section and electron (hole) capture probability coefficient (c_n, c_p) can be given by [3.23]:

$$c_n = \sigma_n \upsilon_{thn} \tag{3.3}$$

$$c_p = \sigma_p \upsilon_{thp} \tag{3.4}$$

Moreover, the electron (hole) emission probability can be related to the electron (hole) capture probability coefficient (e_n, e_p) by the following equations [3.23]:

$$e_n = c_n N_C F_{1/2}\left(\frac{E_T - E_C}{kT}\right) \tag{3.5}$$

$$e_p = c_p N_V F_{1/2}\left(\frac{E_V - E_T}{kT}\right) \tag{3.6}$$

Where N_C, N_V are the effective density of states for electron and holes, E_C, E_V are the conduction and valence band energies and $F_{1/2}$ is the Fermi function of order ½.

$$\upsilon_{th} = \left(\frac{3kT}{m^*}\right)^{1/2} \tag{3.7}$$

$$N_c \equiv 2.M_c.\left[\frac{2\pi m^* kT}{h^2}\right]^{3/2} \tag{3.8}$$

The process of capture and emission of these traps follows the Shockley-Read-Hall theory (SRH) [3.24]. The physical interactions between the free charge carriers and the

generation/recombination mechanisms for the traps located at a particular energy level E_T is shown in Fig. 3.1. The four possible events that can occur for a single level traps located in the energy band of the device [3.23], [3.24]:

(a) The capture of an electron by an empty trap from the conduction band with a capture probability coefficient c_n and electron recombination rate R_n:

$$R_n = c_n.n.N_T(1-f_t) = c_n.n.p_t \tag{3.9}$$

(b) The emission of an electron from the trap energy level to the conduction band with a emission generation rate G_n:

$$G_n = e_n.N_T.f_t = e_n.n_t \tag{3.10}$$

(c) The capture of hole by the occupied trap from the valence band with a hole capture probability coefficient c_p and hole recombination rate R_p:

$$R_p = c_p.p.N_T.f_t = c_p.p.n_t \tag{3.11}$$

(d) The emission of a hole from the empty trap to the valence band with a hole emission probability coefficient e_p and hole generation rate G_p:

$$G_p = e_p.N_T(1-f_t) = e_p.p_t \tag{3.12}$$

Where N_T is the total number of traps and n_T represent the number of occupied traps.

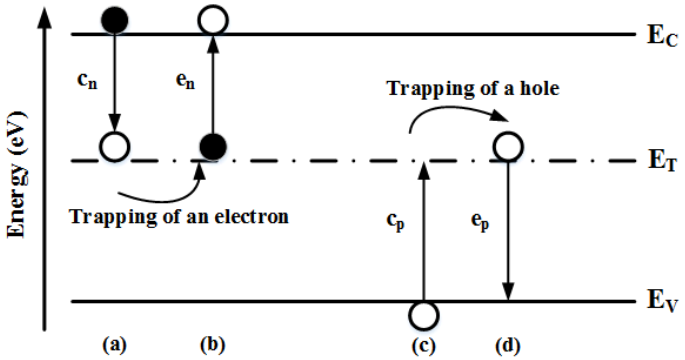


Fig. 3.1. Electron and hole transition processes according to SRH theory.

Therefore, the generation-recombination rate can be given by [3.23],

$$U = \frac{\partial n_t}{\partial t} = N_t \frac{\partial f_t}{\partial t} = (R_n - G_n) - (R_p - G_p) \tag{3.13}$$

$$\frac{\partial n_t}{\partial t} = N_t \left[c_n.n.(1-f_t) + e_p.(1-f_t) - e_n.f_t - c_p.p.f_t \right] \tag{3.14}$$

In steady state conditions, the occupation probability of generation-recombination centers can be given by:

$$\frac{\partial n_t}{\partial t} = N_t \frac{\partial f_t}{\partial t} = 0; f_{t,steady} = \frac{c_n.n + e_p}{c_n.n + e_n + c_p.p + e_p} \tag{3.15}$$

Therefore, the electron emission rate (τ_n) of traps can be obtained by solving the above equations:

$$\frac{1}{\tau_n} = e_n = \sigma_n . A . T^2 \exp\left(-\frac{E_a}{kT}\right) \tag{3.16}$$

Where τ_n represents the electron emission time constant and A is a constant and its corresponding equation is given in (3.17).

With:

$$A = \frac{2 . M_c . \sqrt{3} (2\pi)^{3/2} k^2 m^*}{h^3} \tag{3.17}$$

The capture rate is proportional to the number of electrons in the conduction band, whereas the emission rate has a strong dependence on temperature. This suggests that emission time constant is of several magnitude longer than the capture time constant. In order to obtain the physical properties such as activation energy and the cross section of traps present in the device structure, it is essential to plot the Arrhenius characteristics of traps using any of the measurement technique described in the section 3.1.

3.3. Experimental Characterization

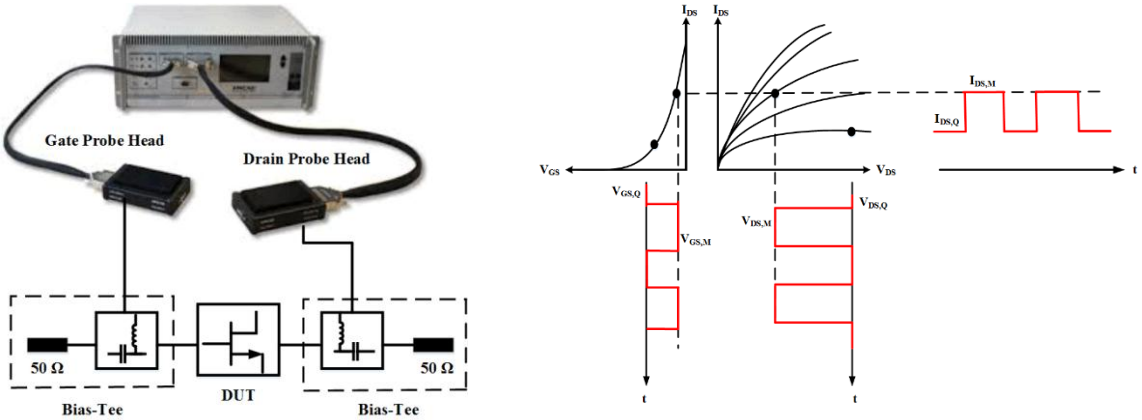
3.3.1. Device Structure

The GaN/AlGaN/GaN HEMTs were grown by metal-organic chemical vapor deposition (MOCVD) on a SiC substrate. The epilayers consist of 1.7-µm thick GaN buffer layer, 22-nm thick AlGaN barrier layer, with Al (m) = 25% followed by a few nm thin GaN cap layer and a 50-nm Si_3N_4 passivation layer. The fabricated devices have a gate length (L_G) of 0.25-µm and widths, W_G of 450 and 600-µm (fingers, n= 6 and 8), whereas the nominal gate-source (L_{SG}) and gate-drain (L_{GD}) spacings are 0.8 and 2.7-µm, respectively. A field-plate is placed from the middle of the gate electrode and extends a distance L_{FP} (field-plate length) of 1-µm towards the drain electrode. Iron (Fe) doping are incorporated in the GaN buffer region of the device.

3.3.2. Pulsed I-V Characterization

The schematic of the pulsed I-V measurement setup used for GaN HEMT characterization is shown in Fig. 3.2 (a). The AMCAD BILT pulsed I-V system consists of power supplies, pulse generators, input/output measurement units, gate and drain probe heads. The gate and drain probe heads are used to provide short pulses, down to 200 ns. Moreover, it is also used to improve the pulse shape even in the case of drastic variation of drain current. The internal

impedances of these I-V probe heads are low (gate – 10 Ω and drain – 0.5 Ω) compared to the conventional high-power pulse pattern generators. The measurement test bench is equipped with a thermal chuck which allows the measurement of I-V for different temperature ranging from -65ºC to 200 ºC. The principle of pulsed I-V measurement is illustrated in Fig 3.2 (b). In general, the measurement are performed under quasi isothermal condition. The gate and drain are pulsed from the initial quiescent bias point (V_{GSQ}, V_{DSQ}) to the measurement bias point (V_{GSM}, V_{DSM}). In order to minimize the influence of self-heating effects on the pulsed I-V measurement, the pulse width for both drain and gate are selected as small as possible. However, the pulse period must be longer than the pulse width. This ensures that the device would return to its steady state conditions. The pulsed IF carried out on the GaN/AlGaN/GaN HEMT grown on SiC substrate. The gate and drain terminals are terminals of the device pulsed at V_{GSQ}, V_{DSQ} = (0 V, 0 V) and the pulse period is set to 900 µs (0.1 % duty cycle).



(a) (b)

Fig. 3.2. (a) Schematic of the pulsed I-V measurement set-up (b). Timing diagram illustrating pulsed I-V measurement principle.

The measurements are carried out for various thermal chuck (T_{chuck}) temperatures ranging between 25ºC and 125ºC. Fig. 3.3 (a) and 3.3 (b) show the measured transfer and output characteristics of the 8×75 µm device at T_{chuck} = 25ºC. Fig. 3.3 (c) and 3.3 (d) show the measured I_{DS}-V_{DS} characteristics at V_{GS} = 0 and -2 V, respectively and for varying T_{chuck} ranging between 25ºC and 125ºC. Fig. 3.4 (a) and 3.4 (b) show the measured input and output characteristics of the 6×75 µm device at T_{chuck} = 25ºC. These measured pulsed I-V characteristics under V_{GSQ}, V_{DSQ} = 0 V conditions are used to calibrate the TCAD simulation model as explained in section 3.5.

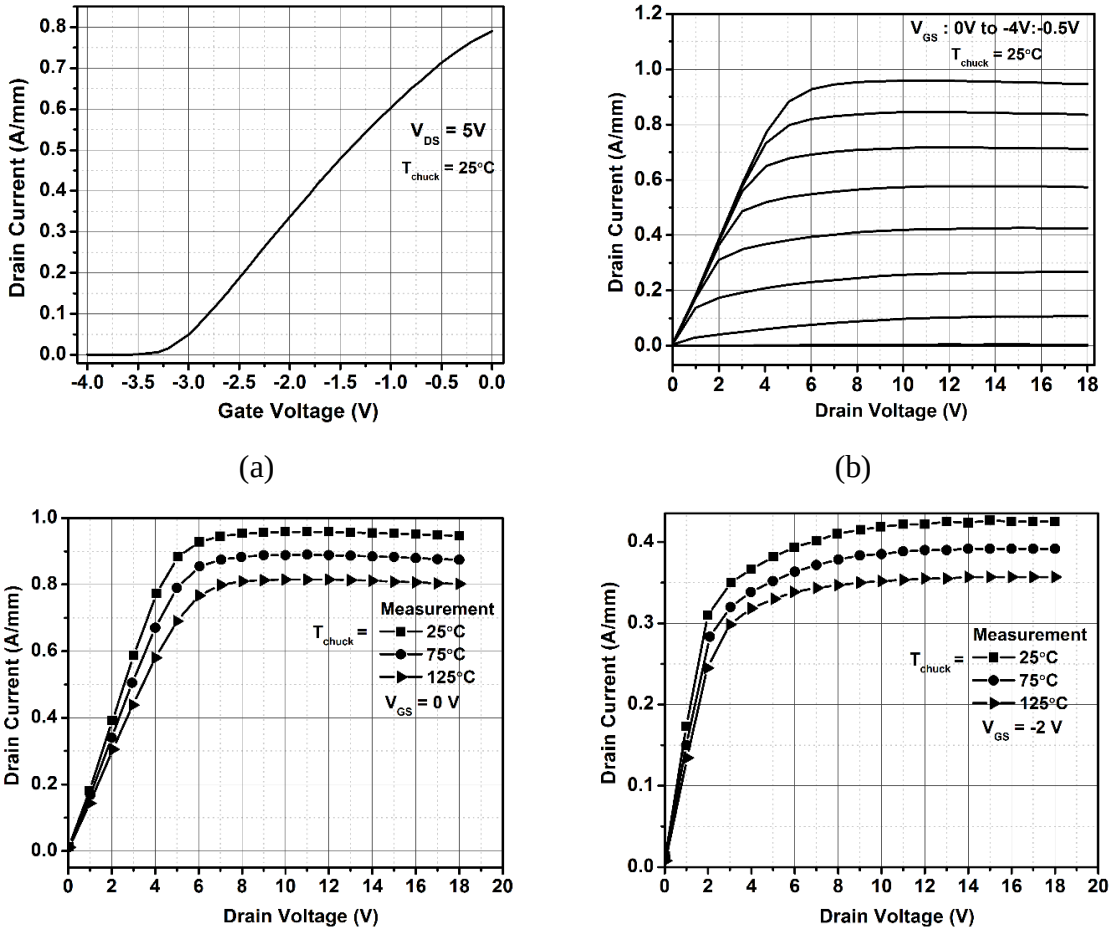


Fig. 3.3. Measured pulsed I-V characteristics of 8×75 µm device at V_{GSQ}, V_{DSQ} = (0 V, 0 V), for varying T_{chuck} ranging between 25ºC and 125ºC and at: (c) V_{GS} = 0 V and V_{GS} = -2 V.

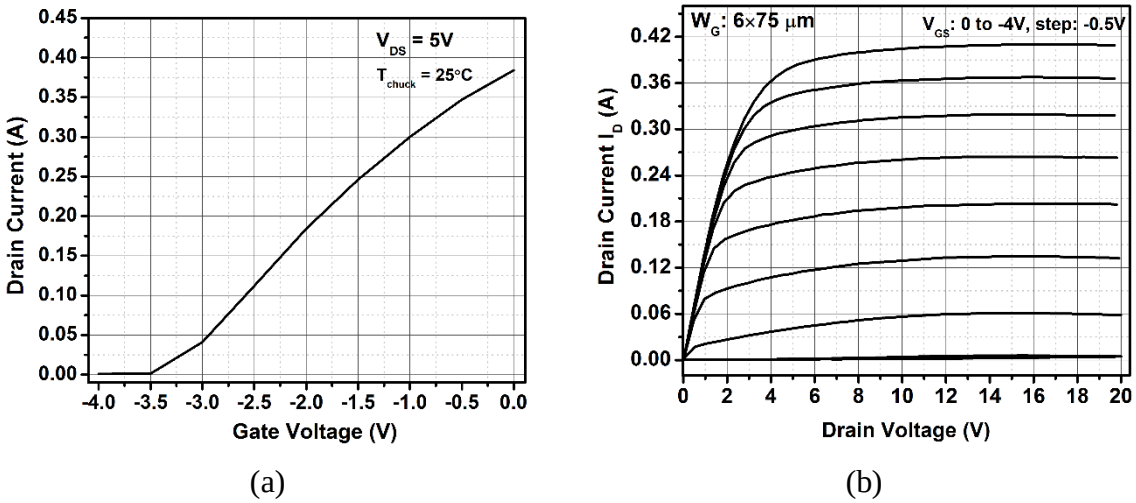


Fig. 3.4. Measured pulsed I-V characteristics of 6×75 µm device at V_{GSQ}, V_{DSQ} = (0 V, 0 V): (a) Transfer characteristics at T_{chuck} = 25ºC (b) Output characteristics for varying V_{GS} between 0 V and -4 V in steps of 0.5 V and at T_{chuck} = 25ºC.

3.3.3. Low Frequency Characterization

The measurement setup used for measuring the LF S-parameters of the device is shown in Fig. 3.5. The Agilent network analyzer (E5061B) is capable of measuring the S-parameters over the frequency range of 5 Hz to 3 GHz. It has its own internal bias tee, which allows measuring up to 100 mA of current and the voltages up to 40 V. In case of a two-port S-parameters measurements, the drain terminal of the device is connected to one port of the E5061B network analyzer, while the gate terminal is biased using an external DC voltage source and connected to the other port. The in-house built low frequency bias tee is used at the gate terminal to connect the active DC power supply and the RF signal port. The device wafer is placed on the measurement bench and the probe station is equipped with a thermal chuck allowing a dynamic temperature range of -65ºC to 200ºC. The on-wafer calibration of the network analyzer is performed using a traditional SOLT method.

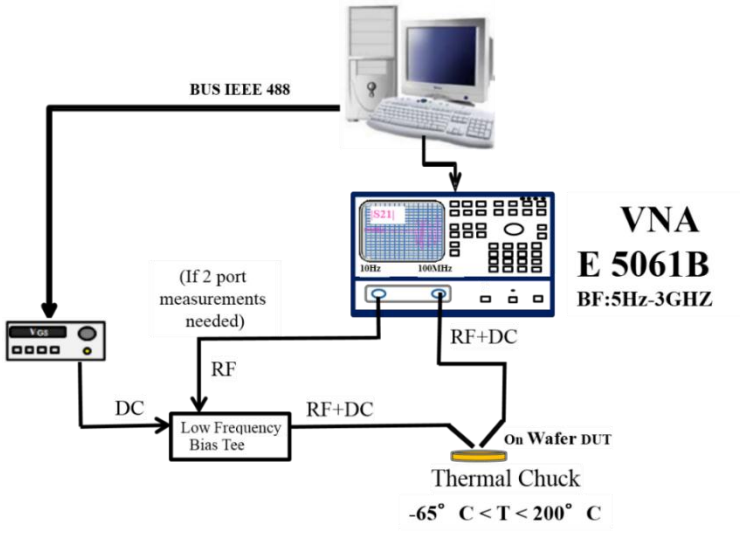


Fig. 3.5. Schematic of the two-port LF S-parameters measurement setup using an Agilent E5061B network analyzer. Frequency range of 10 Hz to 10 MHz has been used for measurements.

3.4. Trapping Investigation using LF Admittance Measurements

3.4.1. Methodology

The LF characterization is used to investigate the trapping mechanism of GaN HEMTs by measuring the low-frequency dispersion of the device output admittance [3.25]–[3.28]. The traps present in the GaN buffer causes the frequency dispersion in the measured admittance characteristics. Moreover, the emission time constant of traps (τ_n) changes with the

measurement temperature. Therefore, by performing the LF output admittance measurements at different temperatures and by using Arrhenius' law, it is possible to extract the physical characteristics such as the activation energy (E_a) and cross section (σ_n) of the traps existing in the GaN buffer.

In the traditional small signal equivalent circuit of the device, the effect of trapping mechanism on the frequency dispersion of output admittance and transconductance can be modeled by using an additional parasitic RC network [3.25] as shown in Fig. 3.6.

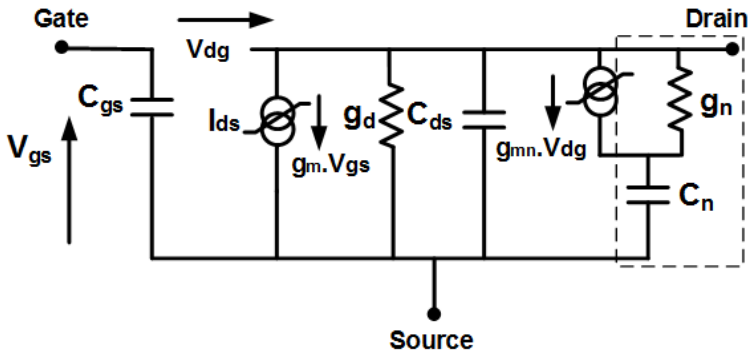


Fig. 3.6. Small-signal HEMT equivalent circuit model including one trap parameters (g_n, C_n).

At low frequencies, the output transconductance and output admittance can be represented by using the following equations [3.25]:

$$Y_{21}(\omega)=\left(g_m-\frac{g_{mn}(\omega\tau_n)^2}{1+(\omega\tau_n)^2}\right)-j\frac{g_{mn}(\omega\tau_n)}{1+(\omega\tau_n)^2} \tag{3.18}$$

$$Y_{22}(\omega)=\left(g_d+\frac{(g_{mn}+g_n)(\omega\tau_n)^2}{1+(\omega\tau_n)^2}\right)+j\frac{(g_{mn}+g_n)(\omega\tau_n)}{1+(\omega\tau_n)^2} \tag{3.19}$$

with $\tau_n=\frac{C_n}{g_n}$

Where τ_n represents the emission time constant associated with the trapping mechanism.

The time constant (τ_n) can be extracted using the frequencies f_{Rinf} and f_{Ipeak} that corresponds to the inflexion points and peak value of the real and imaginary part of Y_{22} parameter, respectively. The corresponding equations can be derived using eqns. (3.18) and (3.19) and are expressed by [3.27]:

$$f_{R\,inf}=f_{Real[Y_{22}]}=\frac{1}{2\pi\sqrt{3}\tau_n} \tag{3.20}$$

$$f_{I,peak}=f_{Imag[Y_{22}]}=\frac{1}{2\pi\tau_n} \tag{3.21}$$

Indeed, it is important to note that the number of inflexion points or the number of peaks

observed in the measured real and imaginary part of Y_{22} parameter signifies the number of traps present in the device, unless the emission time constants of traps are close to each other. The capture time constant of traps is much smaller than the emission time constant and hence, it can be neglected at low frequencies. However, as the temperature increases, the electron emission rate increases, hence the emission time constant decreases which causes the peak value of Y_{22} parameter shift towards higher frequencies. Therefore, the activation energy (E_a) and cross section (σ_n) of the traps can be determined using the Arrhenius equation given below [3.27]:

$$\frac{e_n}{T^2} = \frac{\sigma_n . A_n}{g} \exp\left(-\frac{E_a}{k.T}\right) \tag{3.22}$$

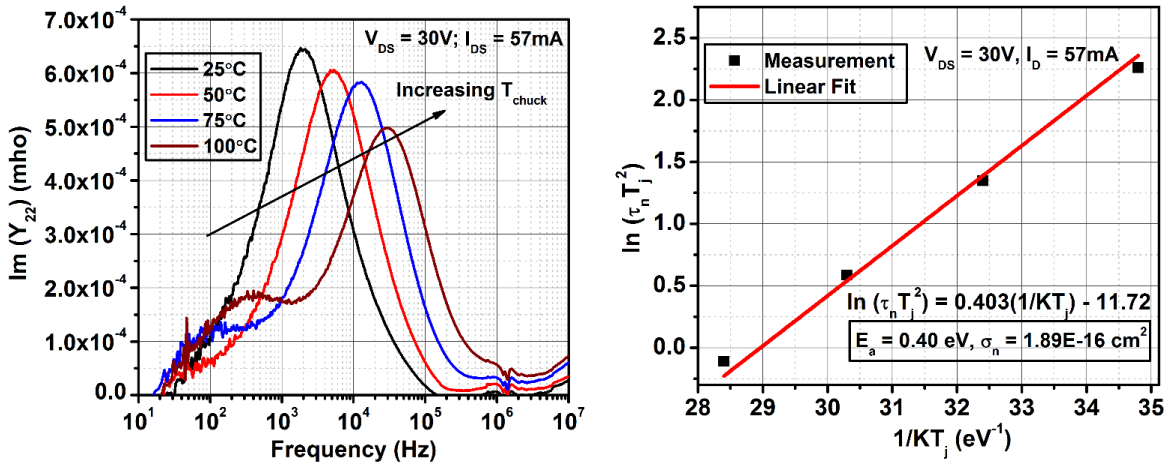
with $A_n = \frac{N_C . V_{th}}{T^2}$ and $e_n = \frac{1}{\tau_n}$

where e_n is the trap emission rate, T is the temperature, σ_n is the capture cross section of traps, N_C is the effective density of states of electrons in the conduction band, V_{th} is the thermal velocity of electrons, g is the degeneracy factor (g =1), E_a is the trap activation energy and k is the Boltzmann constant.

3.4.2. Experimental Results

The low frequency S-parameters measurements in the frequency of 100 Hz to 100 MHz have been carried out using an Agilent E5061B network analyzer. The 8×75 µm device S-parameters measurements have been performed for the bias conditions of V_{DS} = 30 V and I_D = 57 mA (deep class AB operation). This operation mode is selected since it is being widely preferred nowadays for designing RFPAs. The measured LF S-parameters are converted into their equivalent Y-parameters. The emission time constant (τ_n) is calculated at each measurement temperature using (3.21). Then, by using the Arrhenius equation, the plot of $ln\ (\tau_n T^2)$ versus $1/kT$ yields the straight line, whose slope and intercept determine the apparent activation energy and cross section of the traps existing in the device. Fig. 3.7 (a) shows the imaginary part of Y_{22} parameter extracted using LF S-parameters measurements for varying T_{chuck} between 25ºC and 100ºC. Fig. 3.7 (b) shows the Arrhenius plot of traps extracted using LF S-parameter measurements. The apparent activation energy and cross section of the traps determined are 0.4 eV and 1.89× 10^{-16} cm^2, respectively. Therefore, this suggests that traps existing in the device energy band with an apparent activation energy of 0.4 eV below the conduction band. The physical origin of this traps could be related to iron doping present in the GaN buffer [3.29], [3.30]. In general, traps identified using this experimental methodology are more likely to be

located in the GaN buffer. However, it is essential to physically confirm the location of traps in the device using TCAD physics-based device simulations. The TCAD physics based LF-Y_{22} simulations of this device have been explained in section 3.6.4.



(a) (b)

Fig. 3.7. Imaginary part of the 8×75 µm device measured Y_{22}-parameter vs. frequency for the T_{chuck} ranges between 25ºC and 100ºC. Bias conditions: V_{DS} = 30 V and I_D = 57 mA. (b) Extracted Arrhenius plot using Y_{22}-parameter.

3.5. Literature Review on Traps Location and its Activation Energy

In order to understand the physical origin and location of the traps extracted using LF measurements, a comprehensive analysis of the traps characteristics reported in the literature for GaN devices have been reviewed. The majority of the research groups utilizes different characterization techniques to identify the traps existing in the device. However, these measurement techniques provide only qualitative description of trapping mechanism and often lead to conflicting explanations of the physical location of the traps. Therefore, it can be concluded that complete understanding of trapping mechanism and their physical location in the device structure is still under investigation. Table 3.1 shows the summary of the traps characteristics reported in the literature for Fe-doped GaN devices. The summary of the traps characteristics identified for various GaN-devices have been listed in Appendix I.

Table 3.1. Summary of the deep levels (traps) reported in the literature for Fe-doped GaN devices.

Reference	Activation Energy (eV)	Cross Section (cm^2)	Trap Concentration (cm^{-3})	Growth technique	Analyzed samples	Measurement Technique	Interpretation of traps
Umano-Membreno [3.31]	0.21	3.6×10^{-17}	3.1×10^{13}	MOCVD	n-GaN flims (lightly Si doped GaN/Fe-doped GaN buffer	DLTS	Also found in HVPE and RMBE GaN layers
Olena [3.32]	0.23	-	-	MBE	GaN sample	Cathodoluminescence (CL) measurements	Fe-doped GaN
Heitz [3.29]	0.34	-	-	HVPE	GaN samples	Photoluminescence excitation (PLE)	Fe-doped GaN
Olena [3.32]	0.36	-	-	MBE	AlGaN/GaN sample (Al =0.2)	Cathodoluminescence (CL) measurements	Fe-doped AlGaN
Chini [3.30]	0.37 – 0.42	-	-	MOCVD	AlGaN/GaN/SiC HEMTs (Fe-doped)	Drain current turn-on transient measurement	GaN buffer
Umano-Membreno [3.31]	0.535	2.0×10^{-16}	2.7×10^{14}	MOCVD	n-GaN flims (lightly Si doped GaN/Fe-doped GaN buffer	DLTS	Nitrogen antisite defect
Axelsson [3.33]	0.54 – 0.63	-	-	MOCVD	AlGaN/GaN HEMTs (Fe-doped GaN Buffer)	Drain current Transient Measurements (DCTS)	Traps located in the GaN, whose physical properties are influenced by Fe-doping

Bisi [3.34]	0.56	5.0×10^{-15}	-	MOCVD	AlGaN/GaN HEMT (Al =0.25) Fe-doped GaN buffer	DCTS	GaN buffer
Cardwell [3.35]	0.57	1.5×10^{-15}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al=0.3) Fe-doped GaN buffer	Temperature dependent resistance transients (RTS)	Traps located in the GaN, whose concentration is influenced by Fe-doping
A. Chini [3.36]	0.57 0.58 0.59	5.86×10^{-15} 5.13×10^{-15} 2.24×10^{-14}	-	MOCVD	AlGaN/GaN HEMTs	Drain Current Transient Measurements	Fe-doped GaN buffer
Matteo [3.37]	0.63	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Fe-doped GaN buffer)	Drain current Transient (DCT)	GaN buffer, whose properties depends on the concentration of Fe-doping
Silvestri [3.15]	0.66 0.68 0.7	1.0×10^{-13} 4.0×10^{-13} 8.0×10^{-13}	-	MOVPE	AlGaN/GaN/SiC HEMTs (Al =0.22) (Medium/ High/Low Fe-doped GaN buffer)	Transconductance frequency dispersion	Traps located in GaN buffer, whose energy levels and cross sections are influenced by Fe-doping.
Silvestri [3.38]	0.7	8×10^{-13}	-	MOVPE	AlGaN/GaN/SiC HEMT (Fe doped GaN)	Transconductance frequency dispersion	GaN bulk

3.6. Trapping Investigation using TCAD Physical Simulations

3.6.1. Introduction

Physics based simulations offer an efficient way for analyzing the experimental device characteristics. However, in order to make the 2D simulations physically more meaningful, it is essential to calibrate the TCAD physical models used in the simulation to reproduce the experimentally measured characteristics. Moreover, the calibration process is not relatively straightforward. The parameters of interest for the calibration are the polarization charges defined at the hetero-junction interface, surface donors, interface charge, mobility and saturation velocity of the GaN material, Schottky work function of the gate metal and contact resistances of source and drain contacts respectively. Some of these parameters can be independently measured or the parameter values can be taken from the literature. The polarization charges defined at the hetero-junction interface can be computed using the eqns. (2.1) – (2.3) as explained in Chapter 2. The interface charge is used as a fitting parameter and moreover, this interface charge is compensated by the donors-like traps introduced at the surface of the device. Furthermore, it is important to note that the simulation performed with these reported or calculated values could not reproduce the experimentally measured characteristics of our device. Hence, these values can be considered as the reference values for our calibration process. Moreover, each of these parameters has a distinct impact on different regions of the measured I-V characteristics.

The calibration process can be divided into several regions. The initial calibration is performed by adjusting the Schottky gate work function in order to fit the pinch-off voltage in simulation to experimentally measured characteristics. Then, by varying the low field mobility and saturation velocity, the linear and saturation region drain current characteristics are calibrated. Moreover, the AlGaN/GaN HEMT devices are used mainly for high power and high voltage applications due to their excellent high electron drift velocity and large bandgap. This drift velocity would be the limiting factor for device operation under high electric field conditions. Under high electric fields, the carrier velocity is no longer proportional to the electric field strength, but saturates to a finite value. In order to account for the velocity saturation in the simulation, the most commonly used Caughey Thomas field dependent mobility model is used. The relation between the velocity, mobility and the electric field can be expressed by [3.39],

$$\mu_{n,p} = \frac{\mu_{low}}{\left[1+\left(\frac{\mu_{low}.E}{V_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{3.23}$$

Where V_{sat} represents the saturation velocity, μ_{low} is the low-field mobility, $\mu_{n,p}$ denotes the mobility of electrons/holes, respectively and β is the fitting parameter (i.e., 2.9 for electrons in GaN) that controls the smooth transition between the linear and saturation region of the dependence of velocity on the electric field.

The velocity as a function of electric field can be expressed by using the following relation:

$$\upsilon_{n,p} = \mu_{n,p}.E \tag{3.24}$$

Fig. 3.8 shows the variation of electron mobility and velocity as a function of electric field for two different electron saturation velocity values.

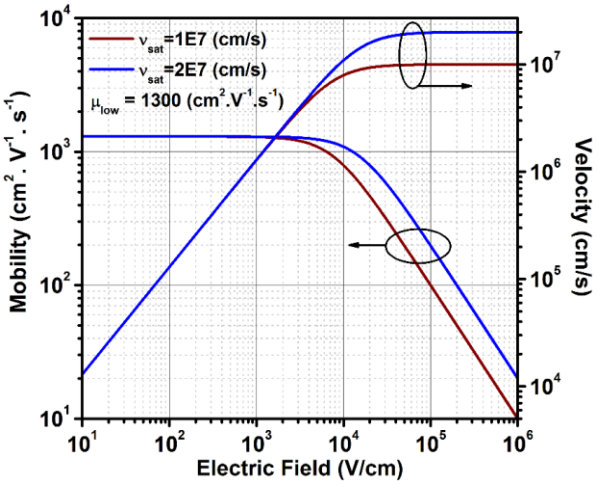


Fig. 3.8. Variation of electron mobility and velocity as a function of electric field using the Caughey Thomas field dependent mobility model. For low electric fields, the mobility is determined by the low-field mobility value and under higher electric fields, the velocity is dependent on the saturation velocity.

The temperature-dependent carrier mobility values are calibrated using a generic model [3.40],

$$\mu_{n,p}(T) = \mu_{low}(T_0)\left(\frac{T}{T_0}\right)^{-(\alpha,\gamma)} \tag{3.25}$$

Where T_0 is 298 K, α and γ are the temperature dependent fitting parameters for electrons (2.3) and holes (2.1), respectively for the GaN material.

3.6.2. Calibration of GaN/AlGaN/GaN HEMT

Fig. 3.9 (a) shows the cross section of the structure used for physical simulations. The nominal thickness of all layers detailed in device structure section are used in the simulation except for the case of SiC substrate. The SiC substrate thickness is assumed to be 3 µm, in order to speed up the simulation time. Moreover, it is determined in the simulation, that any further increase in thickness of the SiC substrate after 3 µm will have no significant effect on the simulated DC characteristics. The electric field induced due to the piezoelectric and spontaneous polarization contributes to the formation of 2DEG sheet density at the AlGaN/GaN hetero-junction interface, even without the requirements for any intentional barrier doping [3.41]. In the absence of externally applied fields, the polarization charges induced are of course, equal in magnitude and opposite in sign to maintain the overall charge neutrality of the device. The theoretical method used for the calculation of polarization charges has been described in Chapter 2. Fig. 3.9 (b) shows the polarization charges defined at each material interface in the physical simulator. The values of σ_1 and σ_2 are ± 1.23× 10^{13} cm^{-2} and -2.0× 10^{12} cm^{-2}, respectively. According to surface donor theory [3.42], the surface donors are responsible for the formation of 2DEG sheet density in GaN HEMT devices. Hence, surface donors (σ_D^+) with a density of 1.0× 10^{13} cm^{-2} and a specified energy level of 0.2 eV below the conduction band are introduced at the GaN-cap/SiN interface. Electron (σ_n) and hole (σ_p) capture cross sections are assumed to be 1.0× 10^{-18} and 1.0× 10^{-20} cm^2, respectively. Fe-doping (p-type) are introduced uniformly in the GaN buffer with a uniform concentration (N_{buffer}) of 3.0× 10^{16} cm^{-3}.

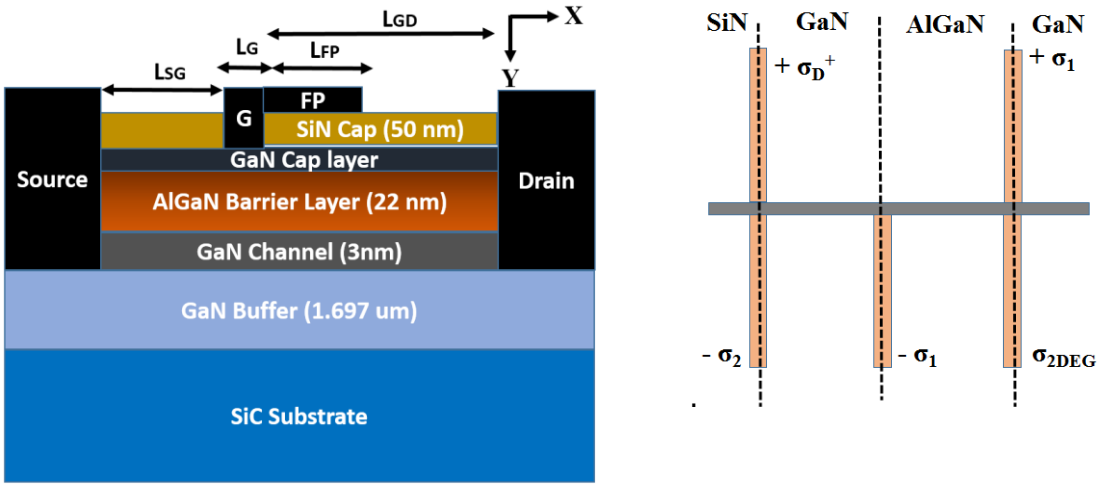
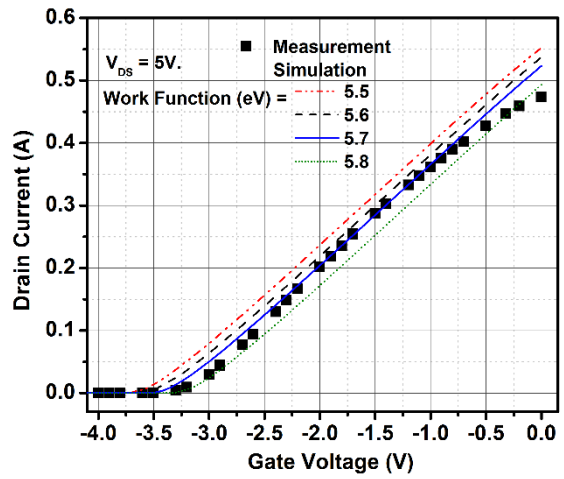


Fig. 3.9. (a) Schematic cross section of the GaN/AlGaN/GaN HEMT structure. (b) Polarization charges defined at each material interface in the TCAD simulation.

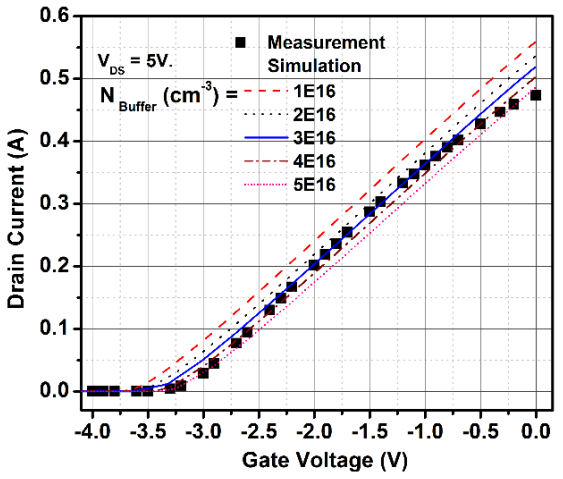
In addition, we consider acceptor-like traps in the GaN buffer whose trap energy is placed at 0.4 eV below the conduction band and the assumed trap concentration (N_{TA}) is 5.0× 10^{16} cm^{-3}. Electron (σ_n) and hole (σ_p) capture cross sections of GaN buffer traps are assumed to be 3.2× 10^{-18} and 1.0× 10^{-20} cm^2, respectively. For the simulation, constant mobility and field dependent mobility models are included for electrons and holes and Shockley-Read-Hall recombination model is used for carrier generation and recombination.

3.6.3. Calibration Results

Fig. 3.10 illustrates the influence of different calibration parameters on the 8×75 µm device simulated I-V characteristics and moreover at the end of this calibration process, the essential device parameters can be extracted. The calibration of each of the physical parameters are repeated several times in order to achieve the best match with the experimentally measured I-V characteristics.



(a)



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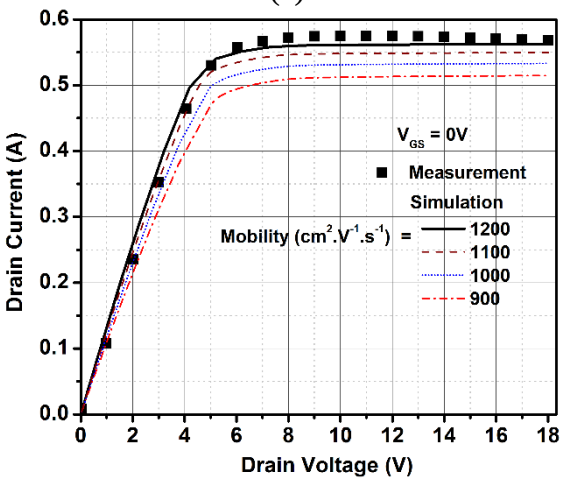
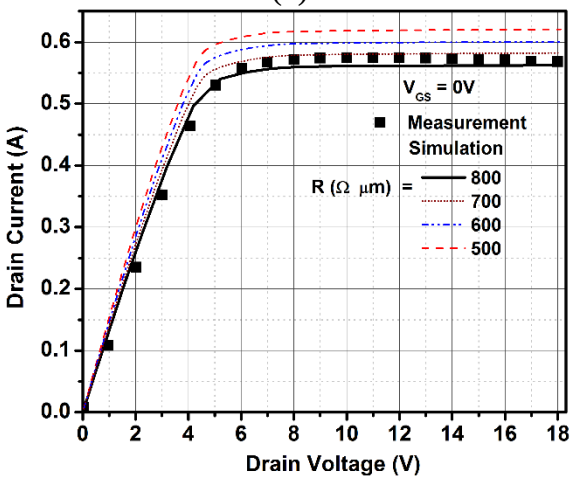
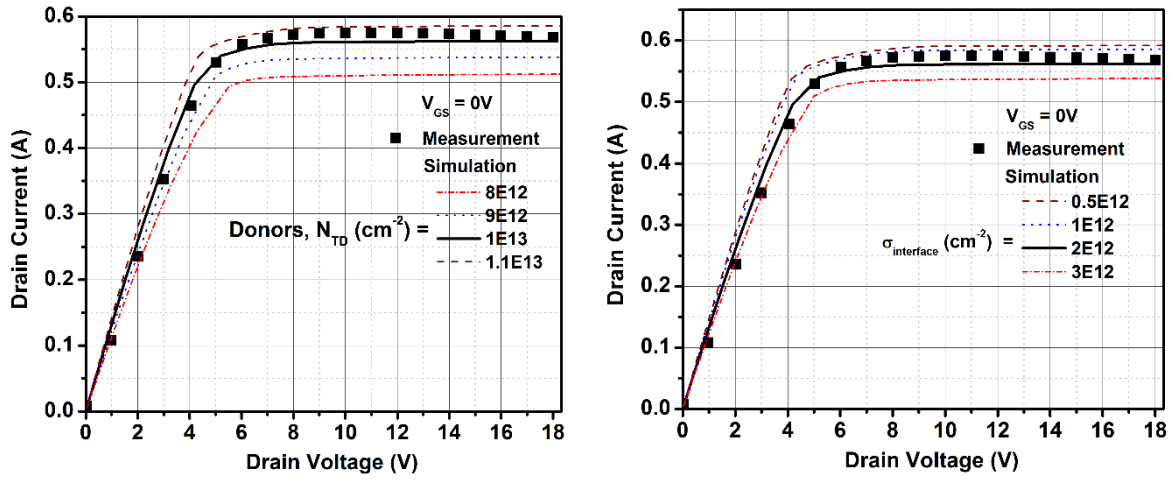


(c)



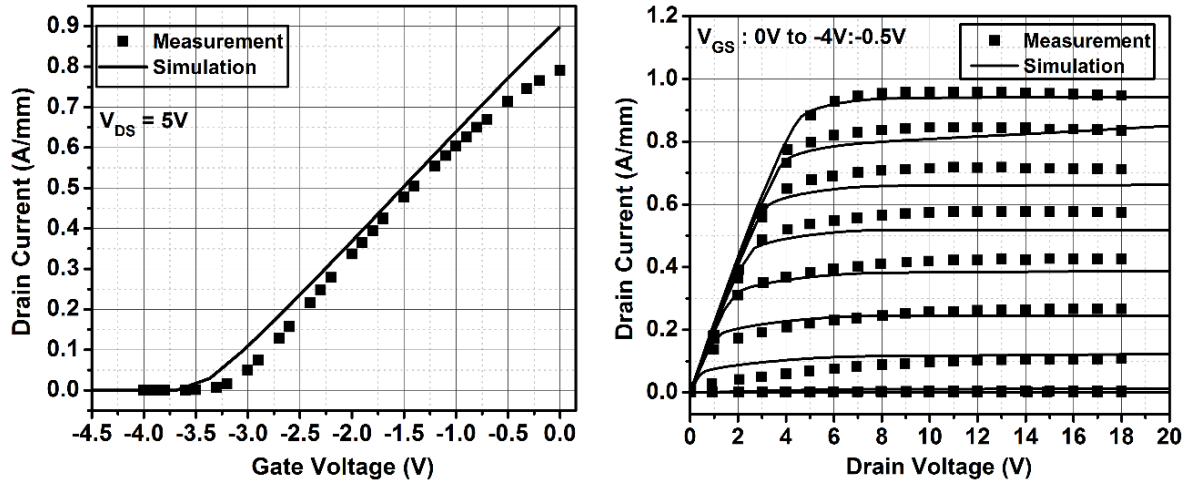
(d)



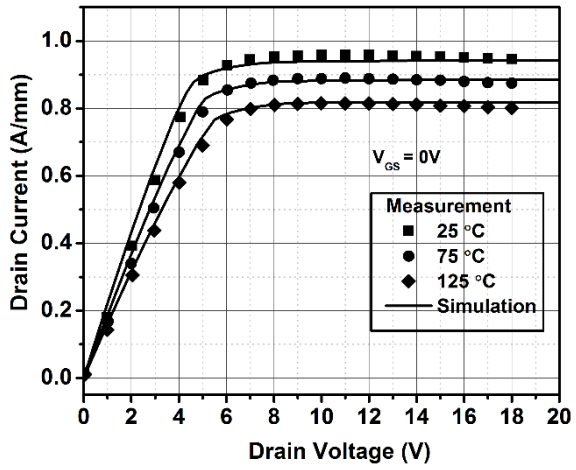
(e) (f)

Fig. 3.10. 8×75 µm device TCAD physical model calibration process: (a) Optimizing the Schottky work function to match the pinch-off voltage ($V_{pinch\text{-}off}$) in experiment to simulation. (b) Influence of Fe-doping concentration (N_{buffer}) on the simulation, N_{buffer} = 3.0× 10^{16} cm^{-3} yields an excellent match with experimental characteristics. At V_{GS} = 0 V: (c) Fitting the linear and saturation region of the I-V characteristics by varying low-field mobility and at fixed saturation velocity. (d) The variation of contact resistance R (Ω. µm) affects the slope of the simulated I-V characteristics. (e) Influence on surface donors concentration on the simulation characteristics. (f) Optimizing the interface charge concentration. $\sigma_{interface}$ = -2.0 × 10^{12} cm^{-2} gives the best match with experimental results.

Fig. 3.11 (a) and 3.11 (b) show the comparison of the measured and simulated transfer and output characteristics of the 8×75 µm device at T_{chuck} = 25ºC.



(a) (b)



(c)

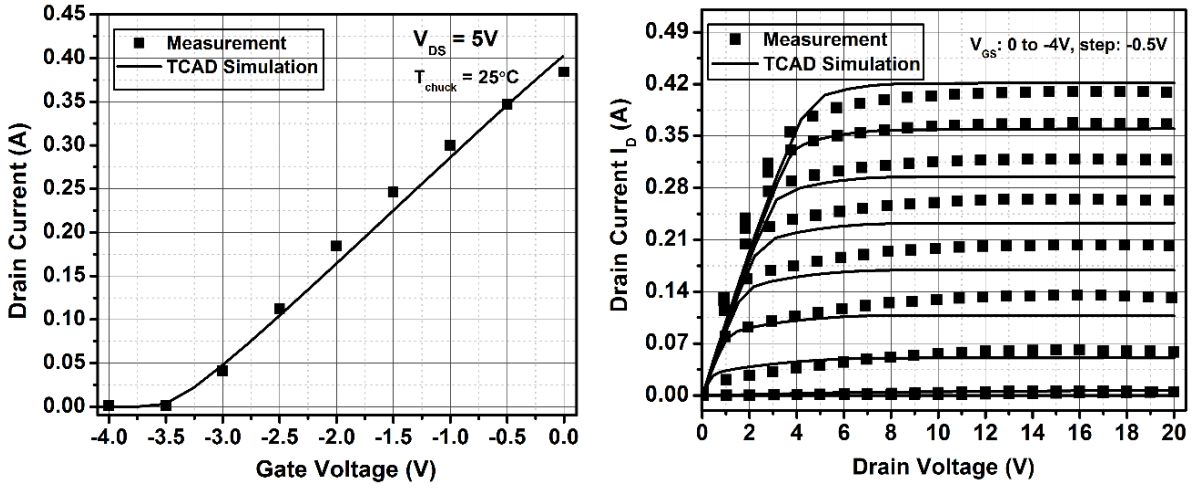
Fig. 3.11. 8×75 µm device: Comparison of the simulated (solid lines) and measured (symbols) I-V characteristics. (a) Transfer characteristics at V_{DS} = 5 V and T_{chuck} = 25°C. (b) Output characteristics for varying V_{GS} between 0 V and -4 V in steps of 0.5 V and at T_{chuck} = 25ºC. (c) Output characteristics for T_{chuck} varying between 25ºC and 125ºC and at V_{GS} = 0 V.

Fig. 3.11 (c) shows the comparison of the measured and simulated I_{DS}-V_{DS} characteristics at V_{GS} = 0 and for varying T_{chuck} between 25ºC and 125ºC. The good agreement between the simulation results and measured data confirms the validity of the TCAD simulation model calibration. The summary of the material parameters used in our simulations is shown in Table 3.2.

Table 3.2. Summary of the material parameters used in TCAD simulations.

Material Property	**Units**	**GaN**	**AlGaN**
Electron Mobility	$cm^2/V\ s$	1200	300
Bandgap	eV	3.50	4.39
Relative permittivity	-	8.9	8.8
Electron affinity	eV	4.0	3.41
Electron saturation velocity	cm/s	2.5×10^7	1.1×10^7
Effective conduction band density of states	cm^{-3}	2.23×10^{18}	2.71×10^{18}
Effective valence band density of states	cm^{-3}	2.51×10^{19}	2.06×10^{19}

The calibrated TCAD simulation model is used to simulate the I-V characteristics of 6×75 µm device and obtained simulation results are compared with the measured pulsed I-V characteristics (Fig. 3.12). Good agreement is achieved between the measurement and simulation results, this confirms that calibrated simulation model is also valid for the 6×75 µm device.



(a) (b)

Fig. 3.12. 6×75 µm device: Comparison of the simulated (solid lines) and measured (symbols) I-V characteristics. (a) Transfer characteristics at V_{DS} = 5 V and T_{chuck} = 25°C. (b) Output characteristics for varying V_{GS} between 0 V and -4 V in steps of 0.5 V and at T_{chuck} = 25°C.

3.6.4. TCAD Low – Frequency Y_{22} Simulations: Identification of GaN Buffer Traps

Using the calibrated TCAD simulation model, LF admittance parameters simulation has been carried out at the bias conditions of V_{DS} = 30 V and I_D = 57 mA. The activation energy of traps extracted using LF measurements are used in TCAD simulations. The self-heating effect of the device has been taken into account by extracting the thermal resistance (R_{TH}) of the device using the method described in [3.43]. The detailed methodology for extracting the R_{TH} of the device has been described in chapter 5. The extracted R_{TH} of the device is approximately found to be 20.42 °C/W. Thus, by knowing the R_{TH} value, the T_{chuck} and the power dissipation (P_{diss}), the junction temperature (T_j) has been estimated for different T_{chuck} and are used in simulations. Fig. 3.13 shows the simulated 8×75 µm device Y_{22} parameter for different electron cross section parameters (σ_n) and for T_{chuck} = 25°C. The σ_n value of 3.2×10^{-18} cm^2 and N_{TA} of 5.0×10^{16} cm^{-3} yields an excellent match between the measured and simulated Y_{22} parameters over the temperature range of 25°C to 125°C. Therefore, these particular values have been used in all the TCAD physical simulations. Fig. 3.14 (a) shows the comparison of the simulated and measured imaginary part of the Y_{22} parameter for the frequency range of 10 Hz to 10 MHz and for various chuck temperatures. The good agreement obtained between the TCAD simulations and measurements confirms the presence of acceptor-like traps in the GaN buffer of the device. This is the first time such a direct comparison between the simulated and measured Y_{22} parameter has been reported for a GaN HEMT.

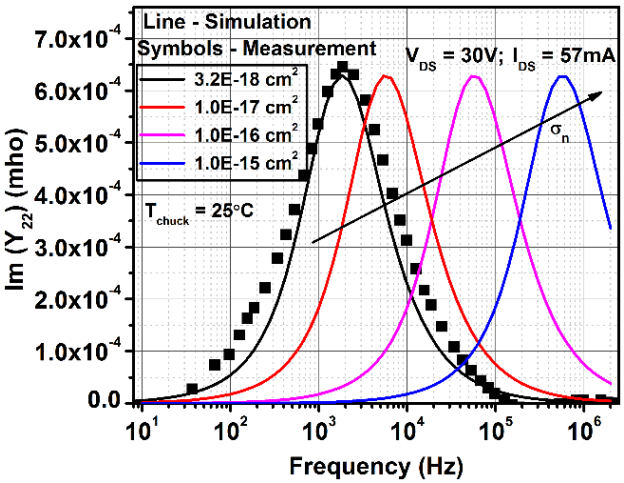
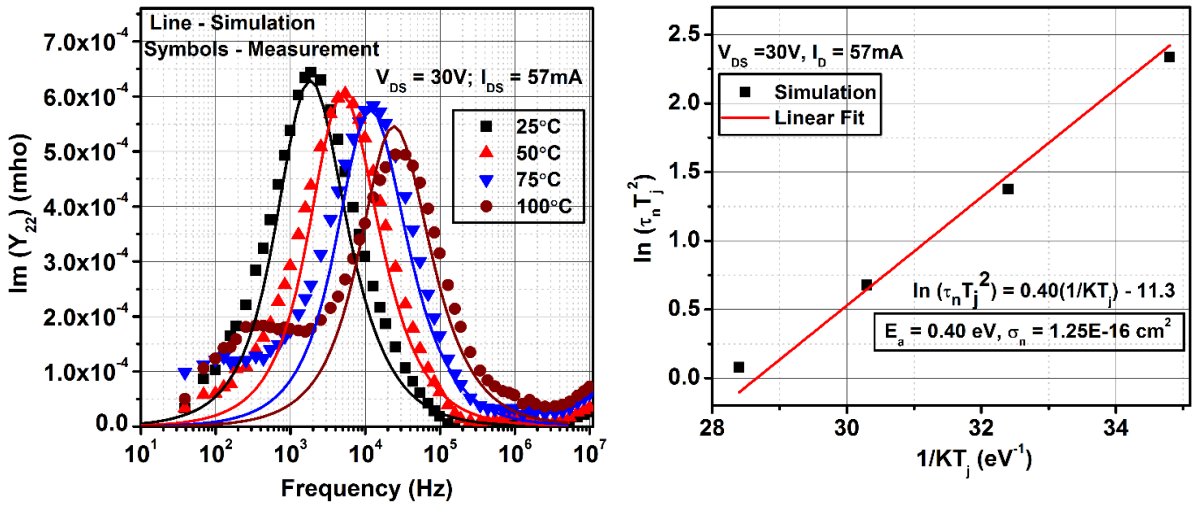


Fig. 3.13. 8×75 µm device: Imaginary part of the simulated (lines) and measured (symbols) Y_{22}-parameter vs. frequency for T_{chuck} = 25°C and for different electron cross section parameters (σ_n). Bias conditions: V_{DS} = 30 V and I_D = 57 mA. Activation energy E_a = 0.4 eV, introduced in the simulation.

Fig. 3.14 (b) shows the Arrhenius plot extracted using the simulated Y_{22} parameter. The extracted trap energy level is 0.4 eV which corresponds to the acceptor trap energy level value introduced in the physical simulation. This study confirms that acceptor-like traps are present in the GaN buffer.



(a) (b)

Fig. 3.14. 8×75 µm device: (a) Imaginary part of the simulated (lines) and measured (symbols) Y_{22}-parameter vs. frequency for different T_{chuck} ranging between 25°C and 100°C. Bias conditions: V_{DS} = 30 V and I_D = 57 mA. (b) Extracted Arrhenius plot using the simulated Y_{22}-parameter.

Furthermore, this study also demonstrates that low-frequency admittance measurement is an effective tool for identifying the traps existing in the GaN buffer of the device.The device is biased into off-state stress conditions (V_{DS} = 50 V and V_{GS} = -4 V, below pinch-off) in order to analyze the electric field profile in the device. The electric field obtained from the TCAD simulation is shown in Fig. 3.15 (a). A horizontal cut is made along the X-axis, at the AlGaN/GaN hetero-junction interface in order to visualize the electric field in the channel. Two peaks are observed, one at the drain side edge of gate terminal and the other at the field-plate edge in gate-drain spacing region. Moreover, the electric field below the field-plate edge is higher than under the drain side gate edge [3.17]. The corresponding ionized trap charge density profile is shown in Fig. 3.15 (b).

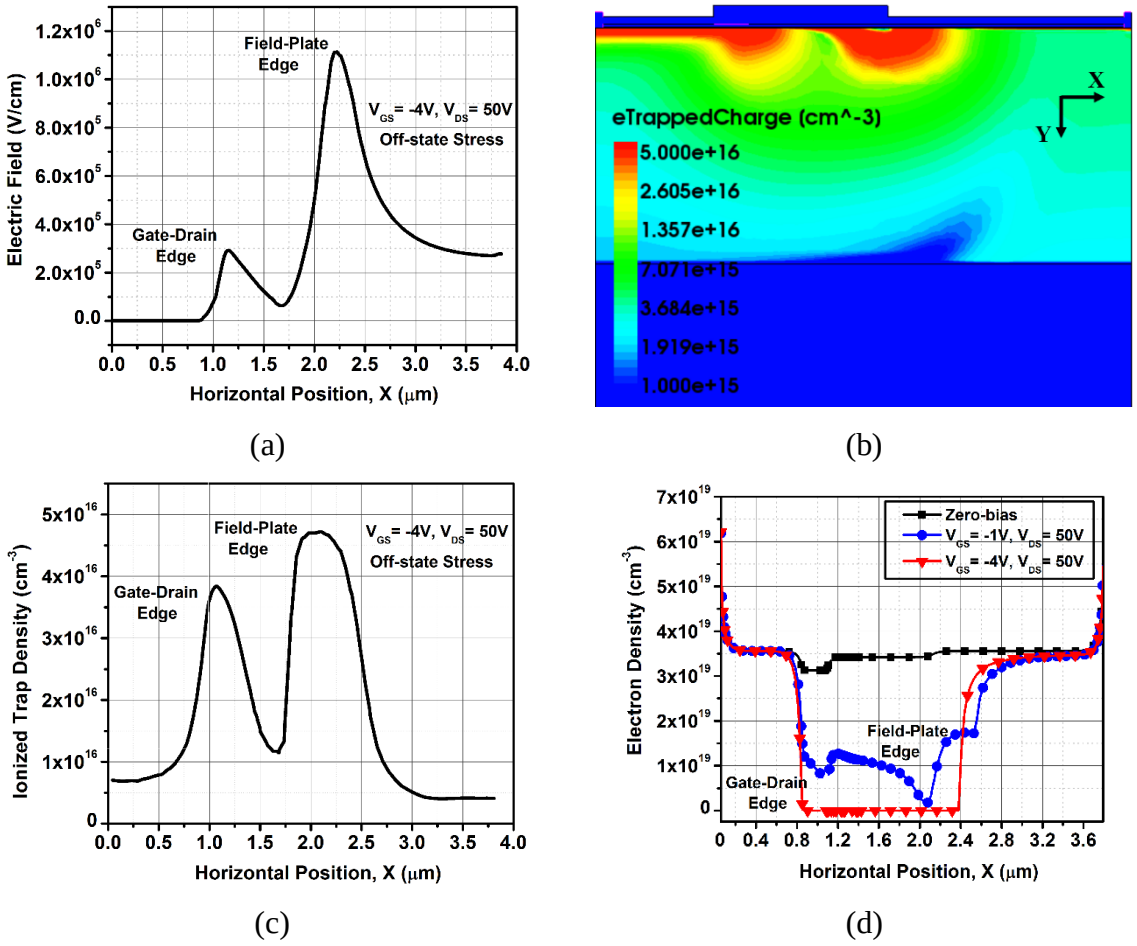


Fig. 3.15. TCAD simulation results of 8×75 µm AlGaN/GaN HEMT device under off-state stress conditions (V_{DS} = 50 V and V_{GS} = -4 V). (a) Electric field profile (b) Ionized acceptor traps density profile (c) Ionized trap density distribution through the GaN buffer layer (d) Electron distribution through the GaN buffer layer for zero bias (V_{DS} = V_{GS} = 0 V) and different device biasing conditions.

The maximum trapping (Fig. 3.15 (b) and (c)) occurs below the field-plate edge where the electric field is maximum. Furthermore, these ionized acceptor traps deplete the 2DEG in the channel. The corresponding simulated electron density in the channel region for different device biases is shown in Fig. 3.15 (d). Using Fig. 3.15 one may conclude that trapping occurs both under the drain side of gate edge and field-plate edge.

3.6.5. TCAD Simulations: Identification of AlGaN Barrier Traps

In this section, we attempt to investigate the influence of barrier traps on the simulated Y_{22} parameter. Fig. 3.16 (a) shows the imaginary part of the simulated Y_{22} parameter when both the acceptor-like and donor-like traps are introduced in the AlGaN barrier.

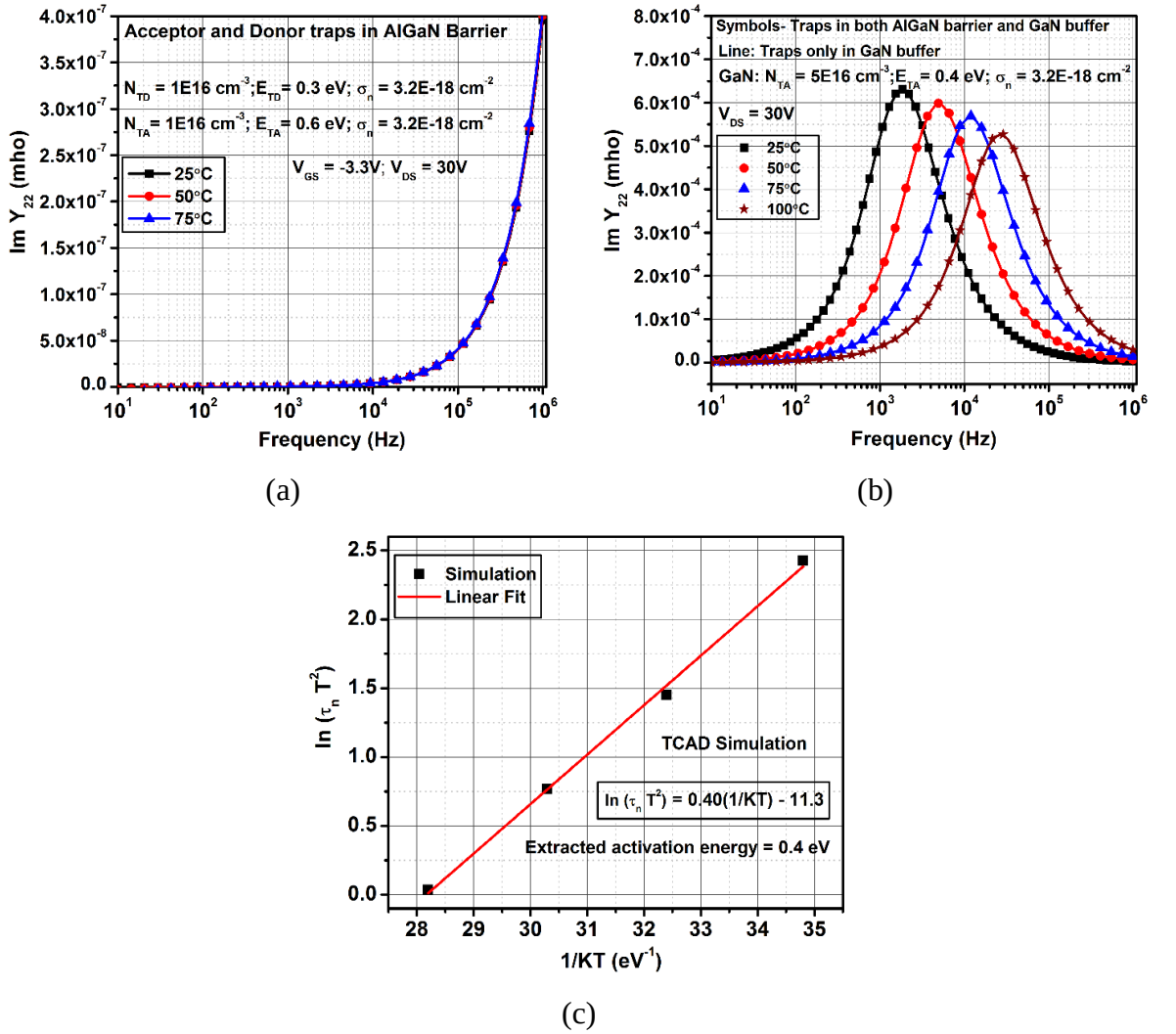


Fig. 3.16. Imaginary part of the simulated 8×75 µm device Y_{22}-parameter vs. frequency for different T_{chuck}. (a) Traps in the AlGaN barrier. (b) Traps in both AlGaN barrier and GaN buffer. (c) Extracted Arrhenius plot using simulated Y_{22}-parameter.

Acceptor-like traps are placed at 0.6 eV below the conduction band whereas donor-like traps are placed at 0.3 eV below the conduction band. Electron and hole cross sections for both these traps are assumed to be σ_n = 3.2× 10^{-18} and σ_p = 1.0× 10^{-20} cm^2 and the assumed trap concentration (N_T) is 1.0× 10^{16} cm^{-3}, respectively. The traps introduced in the AlGaN barrier does not cause any frequency dispersion in the simulated Y_{22} parameter. Moreover, when the traps are introduced in both the AlGaN barrier (both acceptor and donor-like traps) and GaN buffer (E_{TA} = 0.4 eV, N_T = 5.0× 10^{16} cm^{-3}, σ_n = 3.2 × 10^{-18} and σ_p = 1.0× 10^{-20} cm^2), dispersion occurs in the simulated admittance parameter (Fig. 3.16 (b)) and the activation energy value extracted from the Arrhenius plot (Fig. 3.16 (c)) corresponds to the trap energy level value used in the GaN buffer. This result demonstrates that if the traps are present in the AlGaN barrier, low-frequency admittance measurements could not be useful for detecting the traps. However, traps in the AlGaN barrier can be identified via different measurement techniques such as gate lag transients which will be confirmed with the aid of physical simulations in section 3.9.

3.6.6. Influence of Donor Traps on the Simulated Y_{22} Parameter

In order to understand the influence of donor traps on the Y_{22} parameter, donor-like traps are introduced in the GaN buffer, whose concentration is N_T = 1.0× 10^{16} cm^{-3} and the trap energy level is placed at 0.4 eV below the conduction band. The electron and hole cross sections are assumed to be σ_n = 1.0× 10^{-15} and σ_p = 1.0× 10^{-20} cm^2, respectively. Fig. 3.17 shows the simulated Y_{22} parameter for varying temperature ranges between 25ºC and 125ºC and for the gate and drain bias conditions of V_{GS} = -1 V and V_{DS} = 20 V, respectively. For the donor-like traps, the simulated Y_{22} parameter does not show the frequency shift as the temperature increases, instead the peak amplitude increases with temperature. This kind of similar behavior has been observed in our LF measurement of AlN/GaN HEMT device. Fig. 3.18 shows the measured Y_{22} parameter of 4×50 µm AlN/GaN HEMT device for varying temperatures ranging between 25ºC and 125ºC, illustrating the existence of both acceptor-like and donor-like traps. It can be seen that donor-like traps effects are visible only at higher frequencies and therefore, the thermal effects may not significantly influence the measured characteristics. This could explain the reason for no frequency shift observed for donor traps. From the simulations, if the donor-like traps are present in the device, the measured imaginary part of Y_{22} parameter will cause the peak amplitude increase whereas the existence of acceptor-like traps will cause the peak value of Y_{22} parameter shift towards higher frequencies as the temperature increases. This is the first time such an effective way of identifying the type of traps, either acceptor or donor-like traps, using the measured LF admittance parameter, has been reported.

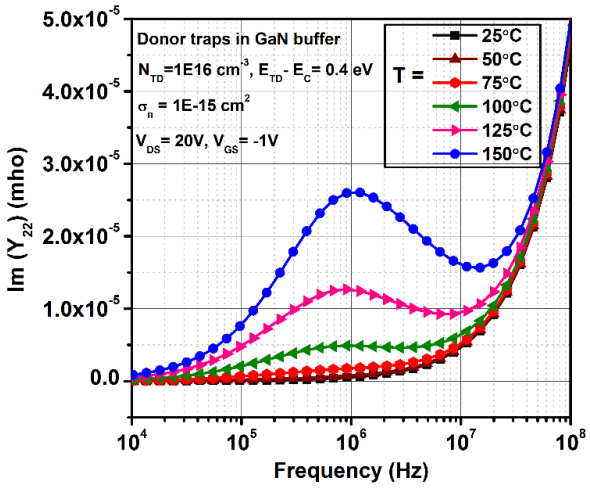


Fig. 3.17. Imaginary part of the simulated 8×75 µm device Y_{22}-parameter vs. frequency for different T_{chuck} and with donor-like traps in the GaN buffer. Bias conditions: V_{GS} = -1 V and V_{DS} = 20 V. Donor-like traps in the device cause the peak amplitude increases as the device temperature increases.

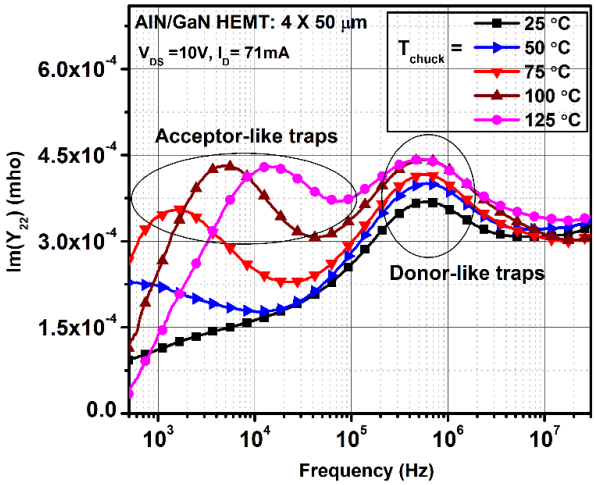


Fig. 3.18. Imaginary part of the measured 4×50 µm AlN/GaN HEMT device Y_{22}-parameter vs. frequency for different T_{chuck}, illustrating the existence of both acceptor and donor-like traps in the device.

3.7. Trapping Investigation using LF Noise Measurements

3.7.1. Introduction

The term "noise" is often related with an unwanted or undesirable random signal that must be reduced as much as possible. This undesired noise component could limit the performance of devices. Therefore, it is of significant importance to understand the origin of these noise sources in order to reduce their level and to improve the performance of the device. Moreover, the origin

of these noise sources are often strongly related with the basic physical mechanisms governing the device operation. Therefore, the study of noise characteristics can provide valuable information about the different physical process occurring in the device. Among various origins of noise sources, some are unavoidable and irreducible noise such as thermal noise, shot noise, and the diffusion noise. However, the low frequency (LF) generation-recombination (GR) noise and 1/f noise of the semiconductor component is a reducible noise [3.44]. Low frequency noise (LFN) characterization is known be to an extremely powerful tool for determining the quality of the device process and studying the device reliability [3.16]. Moreover, it is also useful for identifying the traps existing in the device. The LFN characterization also helps to improve the technological process by tuning the physical parameters of the device such as layer thickness, doping levels, etc., to minimize the noise levels [3.16]. It also helps to model the electrical behavior of the noise sources, which predict the optimal noise characteristics such as phase noise of the oscillator circuits.

The background of noise sources found in semiconductor devices is explained in the next section.

3.7.2. Low Frequency Noise Sources

3.7.2.1. Irreducible Noise Sources

These noise sources contribute to the lower limit of noise level in the semiconductor materials or devices and therefore, they cannot be reduced.

Diffusion and Thermal Noise:

The diffusion noise is related to the diffusion process that results from non-uniform distribution of charge carriers inside the semiconductor material. The physical origin is the fluctuations in the carrier velocity caused by collisions. Moreover, during the diffusion process, the electrons are scattered via collisions with other ionized impurity atoms or with the lattice. These scattering process are completely random and hence the associated instantaneous value of the diffusion current is also random. The noise spectrum of the diffusion noise is relatively flat.

In contrast to diffusion noise, thermal noise is related to the thermal random motion of charge carriers in the semiconductor material. The statistical nature of the scattering of free charge carriers causes random changes in their average carrier velocities and this contributes to random microscopic diffusion currents. Under equilibrium conditions, the charge carrier motion has an average energy of ½ kT.

Under low electric field, the diffusion noise is equivalent to the thermal noise as long as the mobility obeys the following Einstein's relation [3.45]:

$$\frac{D_n}{\mu_n} = \frac{kT}{q} \tag{3.26}$$

Where D_n and μ_n are the diffusion constant and mobility of the charge carriers under low electric field condition. Under these conditions, the power spectral density of diffusion noise is same as that of thermal noise (eqn. 3.33).

Diffusion noise is the more generalized noise process than thermal noise. However, if Einstein's relation holds, diffusion noise becomes thermal noise. The noise power spectral densities can be expressed using [3.45]:

$$S_I = \frac{4kT}{R} \tag{3.27}$$

$$S_V = 4kTR \tag{3.28}$$

Where k is the Boltzmann's constant and Δf is the bandwidth in Hertz.
These noise sources are independent of operating frequency and hence, they are also called as white noise sources.

Shot Noise:

The charge carriers in the semiconductor material or device often flows across a potential barriers. For example, the random motion of electrons or holes in a PN-junction diode or electrons drifting across a potential barrier. These charge carriers cause the fluctuations in current and the corresponding power spectral density of shot noise can be represented using [3.45],

$$S_I = 2qI \tag{3.29}$$

Where q is the electronic charge and I represents the current flowing across the potential barrier. Shot noise is independent of frequency (white noise) and increases proportionally with the current flowing across the potential barrier.

3.7.2.2. Reducible Noise Sources

These noises can be reduced by improving the technological process i.e. by reducing the defects or improving the quality of materials.

1/f Noise:

The *1/f* noise is also called flicker noise [3.45], [3.46], refers to the spectrum that shows a noise power spectral density inversely proportional to frequency ($1/f^{\gamma}$). When γ = 1, the noise is strictly called *1/f* noise. This noise source has been found in different types of materials and systems including semiconductor materials and devices, fluid dynamics and optical systems. Interestingly, this type of noise was identified very early, however the origin of this *1/f* noise is still under investigation. The 1/f noise could be originated due to material and device microscopic degrees of freedom interacting with quantum variables of nano-devices. It could be related to the fluctuations in the conductivity of the material. Moreover, the conductivity of the material depends on both the mobility and the number of free charge carriers, there are two theoretical approaches to describe the *1/f* noise: the McWhorter [3.44] and (number fluctuation model) Hooge [3.46] models (mobility fluctuation model).

Generation-Recombination (GR) noise:

Generation-recombination noise arises due to the existence of traps that randomly capture and emit carriers acting as generation-recombination centers [3.44]. Traps involved in GR noise are located mostly among energy states, between an energy band and a discrete trap energy level in the bandgap of the semiconductor material. Moreover, these traps are generated due to the presence of various defects or impurities in the semiconductor. The traps could either present either at the surface or interface or in the bulk of the material. A trapping-detrapping process results either in generation of excess charge carriers by 'generation' or reduction of charge carriers by 'recombination'. These process cause fluctuations in the number of charge carriers available for current transport. The trapping process also induce fluctuations in the mobility, barrier height and electric field of the semiconductor device.

If there are '*N*' number of charge carriers in the semiconductor device or material at equilibrium condition and if the GR process fluctuates the number of charge carriers (ΔN), the perturbation $d\Delta N$ can be described by a differential equation [3.44],

$$\frac{d\Delta N}{dt} = \frac{-\Delta N}{\tau} + H(t) \tag{3.30}$$

Where τ is the characteristic time constant (lifetime) of recombination of carriers and H(t) is the randomly generated noise source.

For a two-terminal semiconductor sample, the noise power spectral density arising from GR noise can be expressed by [3.44],

$$\frac{S_R}{R^2} = \frac{S_V}{V^2} = \frac{S_N}{N^2} = \frac{\langle \Delta N^2 \rangle}{N^2} \frac{4\tau}{1+(\omega\tau)^2} \tag{3.31}$$

Where R is the resistance of the sample, V is the applied bias voltage, S_R, S_V and S_N are the power spectral densities of resistance, voltage and number of carriers, respectively. This type of spectrum is called Lorentzian noise spectrum. If there are only one trap located in the bandgap of the semiconductor, then the variance can be given by [3.44],

$$\frac{1}{\langle \Delta N^2 \rangle} = \frac{1}{N} + \frac{1}{X_n} + \frac{1}{X_p} \tag{3.32}$$

Where X_n is the average number of traps occupied states and X_p is the average number of empty traps. Thus, the variance approximates the smallest of the quantities N, X_n and X_p.

3.7.3. Low Frequency Noise Characterization Setup

The LF noise of the semiconductor devices can be carried out as equivalent input voltage and current noise sources or in terms of input gate short-circuit current and output drain short-circuit current noise sources as shown in Fig. 3.19. The transistor is modeled as a noiseless transistor with noise current sources at both the ports and their corresponding input and output noise spectral densities are denoted as SI_{in} and SI_{out}, respectively. In order to measure the noise current sources, different setups have been proposed in the literature [3.47]. It is based on either connecting the voltage amplifiers (VAs) or transimpedance amplifiers (TAs) at the transistor terminals and by accounting for the input and output impedances and biasing conditions. Figure 3.20 shows the simplified schematic of two available setups [3.47] to measure the LF noise of the semiconductor devices.

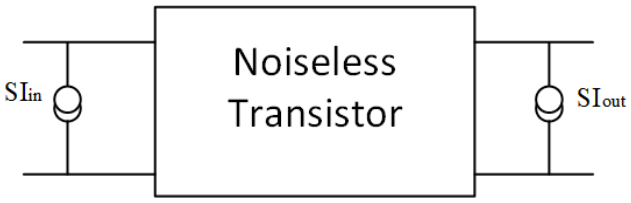
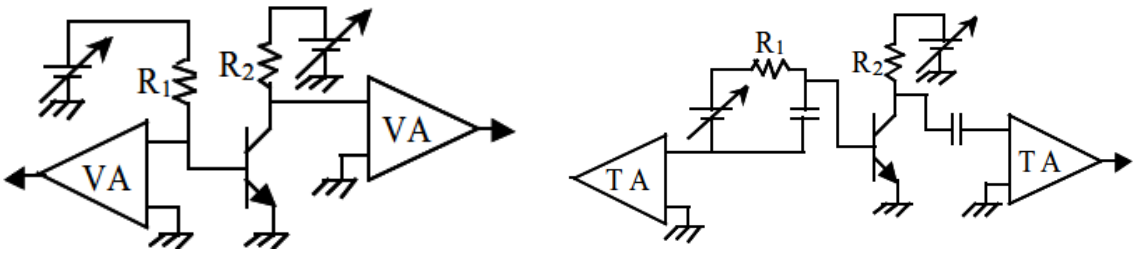


Fig. 3.19. Noise Model of the transistor

In Fig. 3.20 (a), VAs are used and hence the measured noise current sources are converted into its equivalent voltage noise through the measurement resistors, R_1 and R_2 connected at the input

or output terminals. In Fig. 3.20 (b), noise sources are supposed to be drawn completely by the TA's. The bandwidth of these two amplifiers used are different. The TA bandwidth starts at DC, whereas the VA frequency begins only from a few hertz.



(a) (b)

Fig. 3.20. LF Noise Measurement setup [3.45] (a) Voltage amplifiers method (b) Trans-impedance amplifiers method.

The complete setup for noise characterization of GaN HEMT device using the voltage amplifiers is shown in Figure 3.21. The noise voltages generated by the voltage amplifiers are measured using the HP89410A vector signal analyzer. The vector signal analyzer uses the fast Fourier transforms (FFT) and it allows the power of the signal measured either in the frequency or time domain [3.16]. The bias tees are connected in order to avoid the unnecessary oscillations in the RF band. By characterizing the bias tees connected at the input and output terminals of the transistor, the measured power spectral densities SV_{in} and SV_{out} are related to the short circuit noise power spectral densities SI_{in} and SI_{out} of the transistor. In order to avoid the influence of one noise on another, a large value of capacitance (30-mF) is connected at the In or Out node, while measuring the noise at the other terminal.

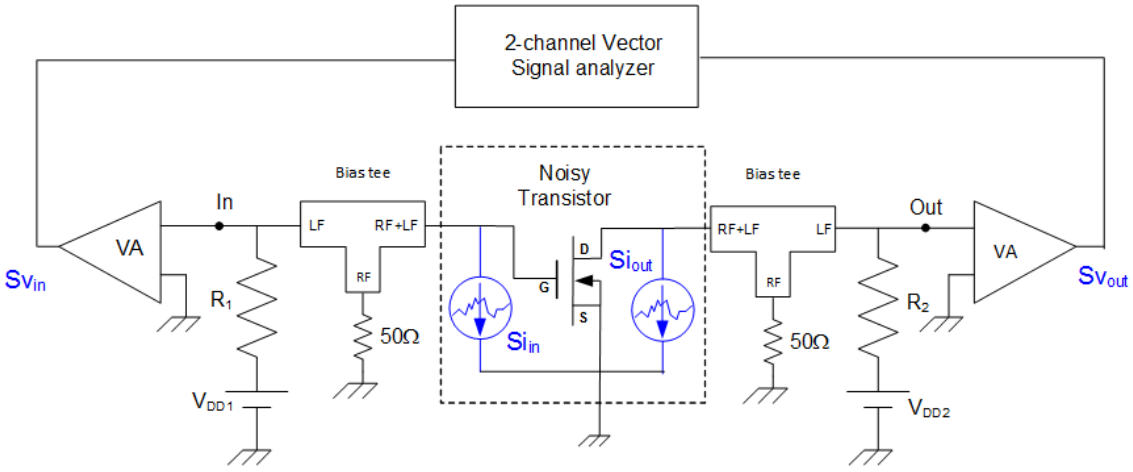


Fig. 3.21. The complete setup for Noise Characterization [3.16].

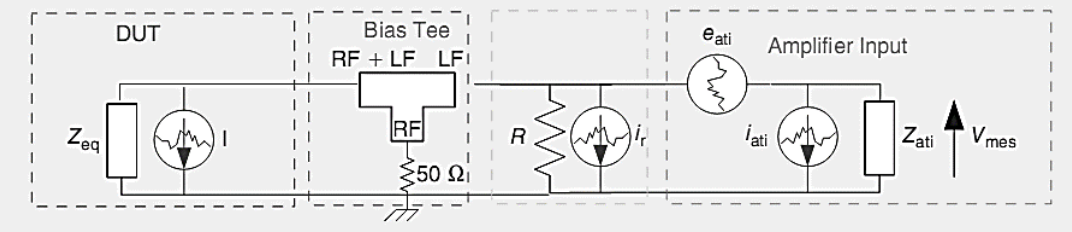


Fig. 3.22. Equivalent circuit representation of LFN measurement [3.16].

The equivalent circuit representation of the complete noise measurement setup is shown in Figure 3.22. The impedance of the DUT is represented by Z_{eq} (at the input or output) and it has its equivalent short noise current I (I_{in} or I_{out}). The bias tees are characterized by their corresponding linear matrices, R will be either R_1 or R_2 depending on the measurement configuration and i_r is the associated thermal noise source. The voltage and current sources of the voltage amplifiers used for the measurement are e_{ati} and i_{ati}, whereas Z_{ati} is its equivalent input impedance. By using the Thevenin – Norton equivalent circuits and assuming that the bias resistor, R generates only thermal noise, the measured voltage noise spectral density is related to the current noise spectral density by using [3.16]:

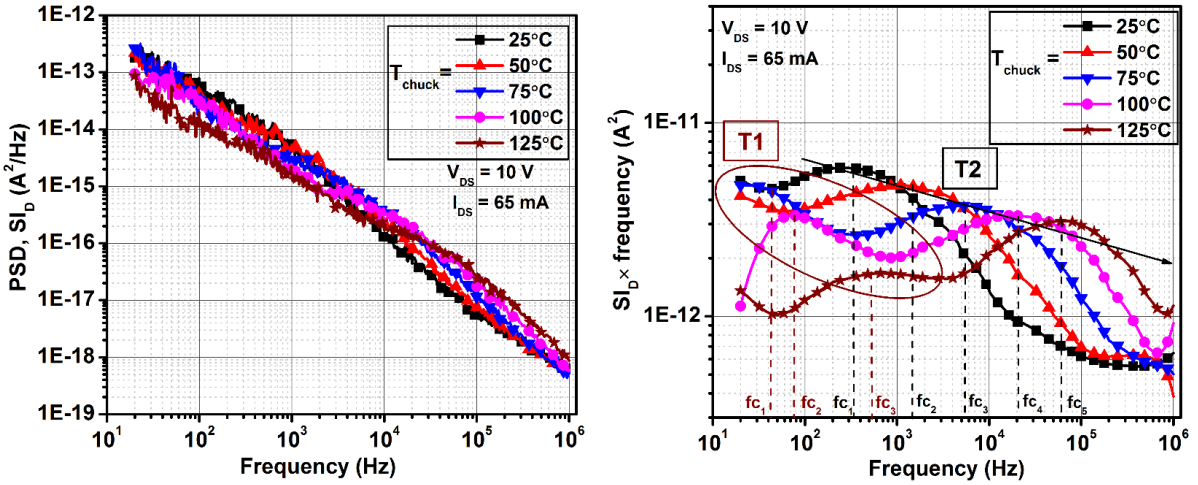
$$S_I = S_{V\_meas}\left|\frac{Z+Z_{ati}}{Z\times Z_{ati}}\right|^2 - \frac{S_{e_{ati}}}{|Z|^2} - 2\times R\left[\frac{e_{ati}\times i^*_{ati}}{Z}\right] - S_{i_{ati}} - S_{i_r} \tag{3.33}$$

Where $Z=Z_{eq}/R$, e_{ati}, i_{ati} and Z_{ati} are the voltage, current noise sources and impedances of the voltage amplifier. S_{V_meas} and S_{ir} are the measured noise voltage spectral density and the thermal noise spectral density associated with the bias resistor R, respectively.

3.7.4. Low Frequency Noise Measurement Results

The low-frequency noise measurements of 6×75 µm GaN/AlGaN/GaN HEMT on SiC substrate have been performed at various chuck temperatures and over the frequency range of 20 Hz to 1 MHz. The device is biased under class AB operating conditions: V_{DS} = 10 V and I_D = 65 mA. The noise floor of the measurement test-bench is 3.0×10^{-27} A^2/Hz at 1 kHz and 7.0×10^{-27} A^2/Hz at 100 kHz, respectively. The output noise voltage spectral density are measured using the noise test-bench shown in Fig. 3.21 and the corresponding noise current spectral density obtained using (3.33) are shown in Fig. 3.23 (a). It can be noticed that 1/f noise dominates at low frequencies whereas the GR noise dominates at higher frequencies. In order to distinguish GR noise from 1/f noise and white noise, the measured output noise spectral density is multiplied by frequency and the corresponding plot obtained for different temperature ranging between 25ºC and 125ºC is shown in Fig. 3.23 (b). It is important to note that there are two trap levels

(T1 and T2) located in the device. The trap level, T1 remains invisible for lower chuck temperatures and, visible only for T_{chuck} > 75ºC whereas the trap level T2 is observable at all measurement temperatures. The characteristics time constant of the GR noise can be obtained from the corner frequency at which 1/f noise crosses the Lorentzian spectrum. Moreover, the 1/f noise is independent of chuck temperature while GR noise is thermally dependent.



(a) (b)

Fig. 3.23. 6×75 µm device measured noise characteristics for various T_{chuck} ranging between 25ºC and 125ºC and under the biasing conditions of V_{DS} = 10 V and I_D = 65 mA: (a) output noise power spectral density vs. frequency and (b) output noise power spectral density multiplied by frequency.

When the temperature increases the peak value of the Lorentzian spectrum shifts toward higher frequencies due to the thermal dependent behavior of GR noise. This allows the extraction of the cut-off frequency for each measurement temperature associated with the GR noise in the device. Thus, the activation energy (E_a) and cross section (σ_n) of these trap levels can be obtained using the Arrhenius equation. Fig. 3.24 shows the summary of the trap levels extracted using LF noise measurements along with the previously reported data [3.28], [3.33], [3.35]–[3.38], [3.48] by several research groups for the case of Fe-doped GaN buffer HEMT devices. The apparent activation energies of the trap levels determined are 0.57 (T1) and 0.51 (T2) eV, respectively. The corresponding cross sections determined are 4.96×10^{-15} and 2.13×10^{-16} cm^2, respectively. The physical origin of these trap levels could be related to the Fe-doped GaN buffer. Moreover, the extracted activation energies of these trap levels are in excellent agreement with the already reported [3.33], [3.34], [3.36], [3.49] values of Fe-doped GaN HEMT devices.

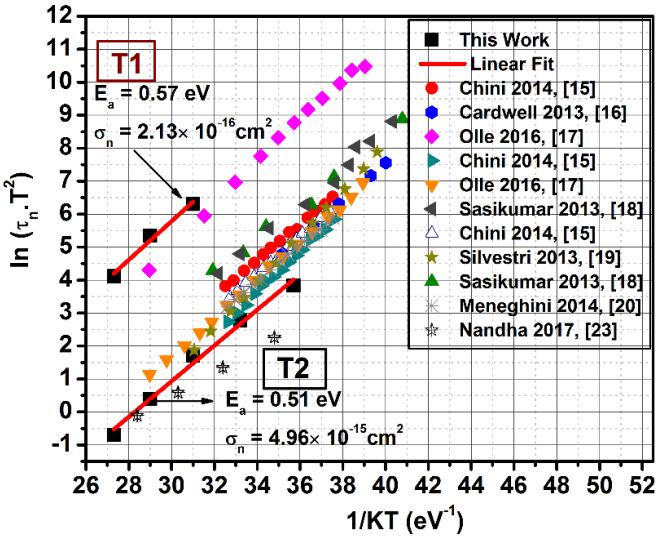


Fig. 3.24. Summary of the trap levels extracted using LF drain noise measurements and previously reported literature data. Two trap levels are identified with an apparent activation energies of 0.51 and 0.57 eV, respectively.

3.7.5. Intepretation Based on Physical TCAD Simulations

In order to identify the physical location of these traps in the device structure, two-dimensional physical simulations have been performed using the schematic structure shown in Fig. 3.9. The polarization charges defined in section 3.6.2 have been used in noise simulations. Two traps are introduced in the GaN buffer which is close to the GaN channel region. It can be seen from the Fig. 3.15 (b), when the traps are uniformly distributed throughout the GaN buffer region, only the region close to the channel (approximately 0.45-µm thickness) is actively involved in trapping phenomenon. Therefore, in our noise simulations, the GaN buffer region is divided into three sections as shown in Fig. 3.25.

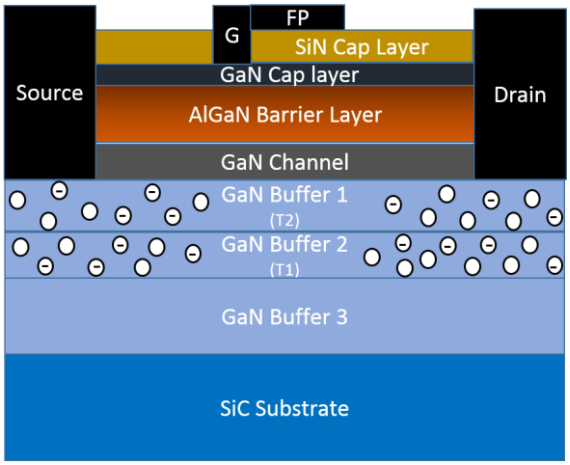
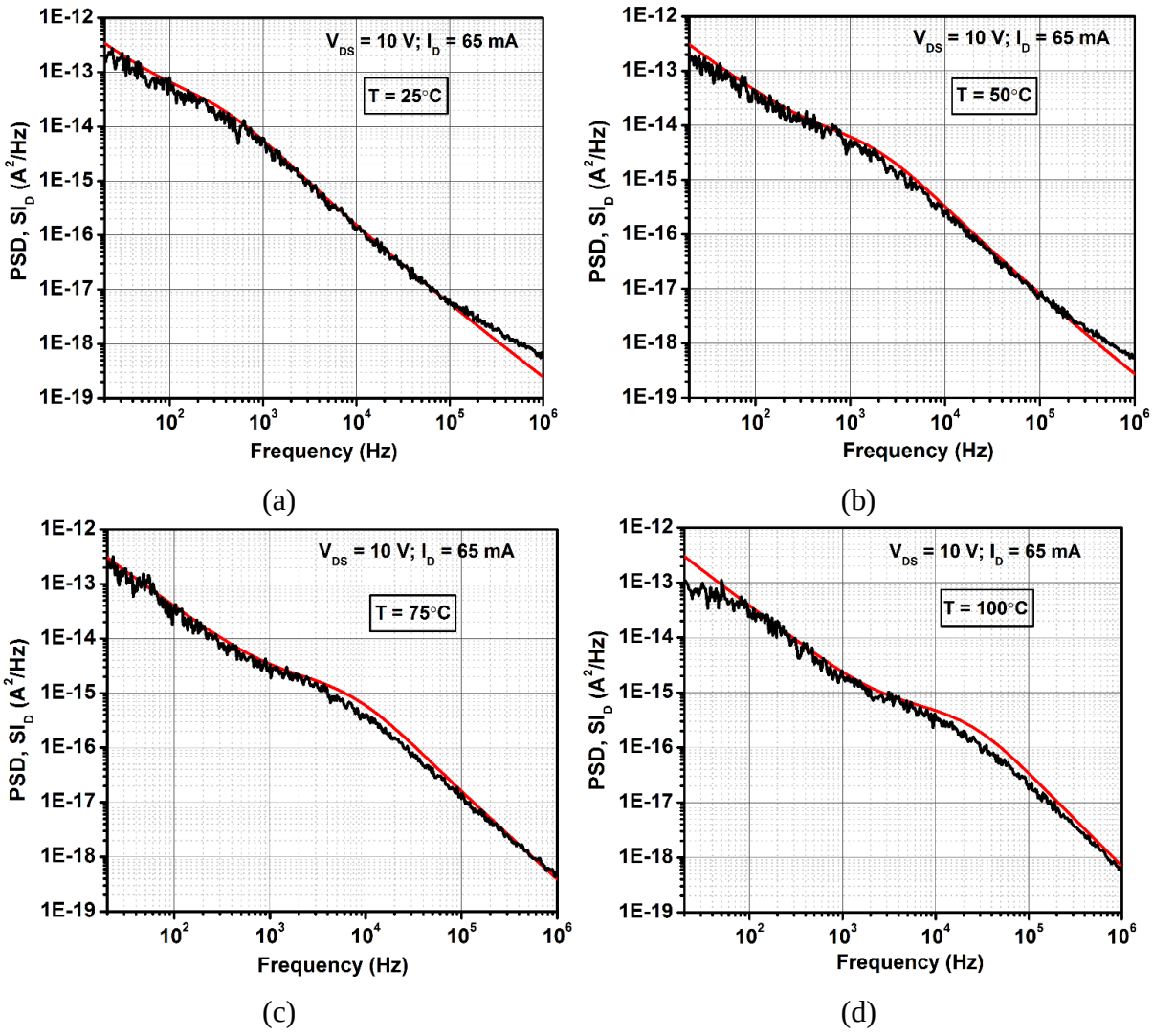


Fig. 3.25. Cross section of the device structure used for TCAD noise simulations.

The thickness of the first two sections are 0.211-µm each, and the third section is 1.275-µm, respectively. In the first section, acceptor-like traps with a density of 5.0× 10^{16} cm^{-3}, having an energy level of 0.51 eV (T2) below the conduction band are introduced. Electron and hole capture cross sections of traps are assumed to be 5.0× 10^{-16} and 1.0× 10^{-20} cm^2, respectively. In the second section of GaN buffer, acceptor-like traps having a concentration of 5.0× 10^{16} cm^{-3} and at the specified energy level of 0.57 eV (T1) below the conduction band are defined. Electron and hole capture cross sections of traps are assumed to be 2.0× 10^{-16} and 1.0× 10^{-20} cm^2, respectively.



(a) (b)

(c) (d)

Fig. 3.26. Comparison of the simulated (red line) and measured (black line) LF drain noise power spectral density for different temperatures ranging between 25ºC and 100ºC. Two trap levels are introduced in the GaN buffer with an apparent activation energies of 0.51 and 0.57 eV, respectively.

Fig. 3.26 shows the comparison of the simulated and measured output drain noise power spectral density (PSD) at different temperatures ranging between 25ºC and 100ºC. Good agreement has been achieved between TCAD physical simulation and measurement, confirms that these two traps are located in the GaN buffer (close to the GaN channel). This is the first time such a comparison between the simulated and measured drain noise spectral density has been reported for the GaN HEMT devices. Fig. 3.27 shows the comparison of the simulated and measured output noise spectral density multiplied by frequency curve for different temperatures ranging between 25ºC and 100ºC.

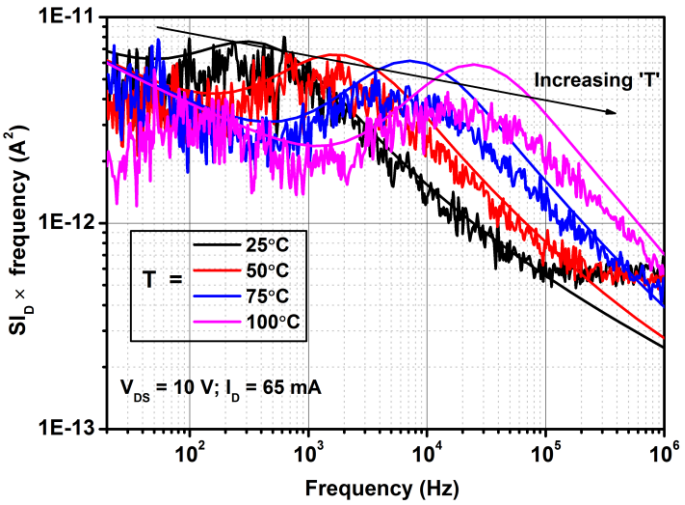


Fig. 3.27. Comparison of the simulated (solid line) and measured (curvy line) LF drain noise PSD multiplied by frequency for different temperatures ranging between 25ºC and 100ºC.

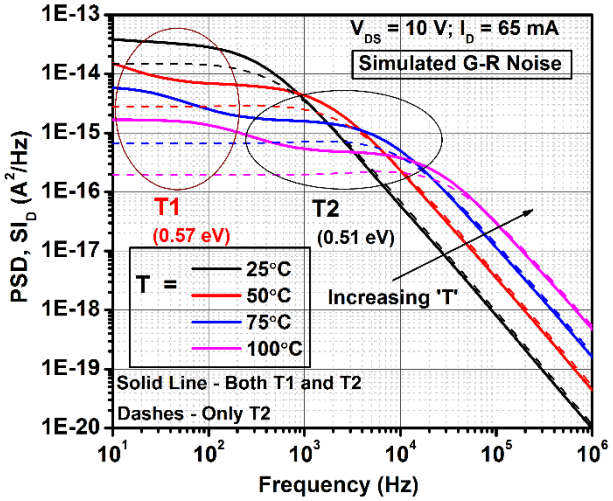
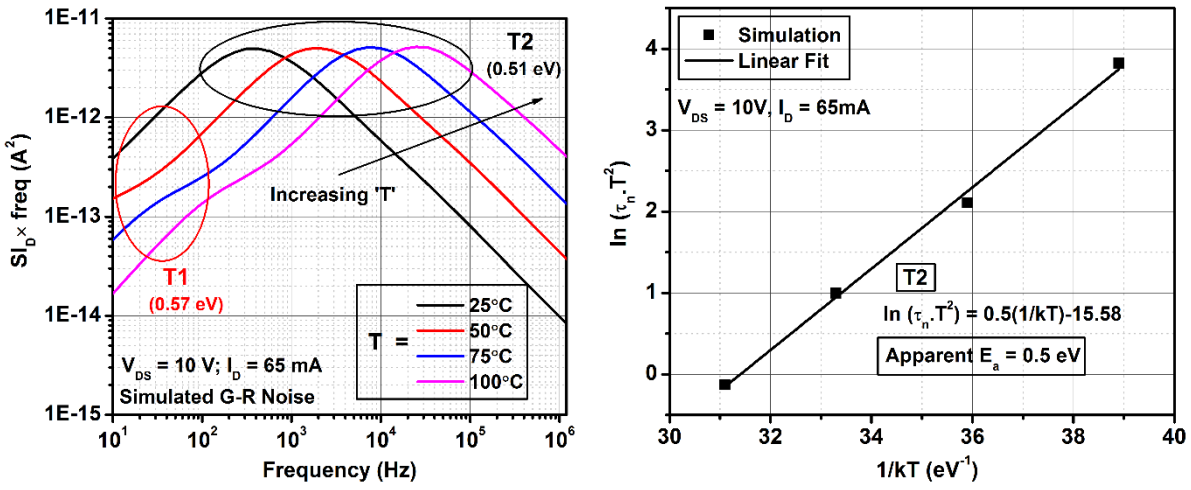


Fig. 3.28. TCAD simulation results of G-R noise for various temperatures illustrating the existence of two traps in the device.

Fig. 3.28 shows the simulated output generation-recombination noise for various temperatures, with and without involving the T1 in the simulation. It is evident from the simulation plot that T1 is visible only for temperatures greater than 50ºC whereas the second trap (T2) is noticeable at all temperatures. The T1 related dispersion in the noise characteristics occurs at very low frequencies and hence this trap is clearly observable only at higher temperatures. Fig. 3.29 (a) shows the simulated output GR noise spectral density multiplied by frequency curve, considering two traps in the GaN buffer and for the temperature ranging between 25ºC and 100ºC. The Arrhenius plot for T2 is extracted using Fig. 3.29 (a) and the corresponding plot is shown in Fig. 3.29 (b). The extracted activation energy of T2 is 0.5 eV, corresponds to the trap energy level of 0.51 eV introduced in the GaN buffer. Therefore, this simulation study confirms that two acceptor-like traps are present in the GaN buffer. Traps with activation energy of 0.51 eV are located close to the GaN channel in the GaN buffer and the traps having an activation energy of 0.57 eV are just located below the 0.51 eV traps. Furthermore, this simulation study also demonstrates that low-frequency noise measurement is another effective tool similar to LF-admittance measurement for characterizing the traps existing in the GaN buffer.



(a) (b)

Fig. 3.29. (a) Simulated GR noise power spectral density multiplied by frequency for various operating temperatures ranging between 25ºC and 100ºC (b) Arrhenius plot extracted for T1 using simulated GR noise spectral density.

3.8. Trapping Investigation using DCTS Measurement

3.8.1. DCTS Drain Lag Measurement

Drain current transient spectroscopy (DCTS), also known as current-mode Deep Level Transient Spectroscopy (I-DLTS) is a powerful transient measurement technique, which can be used to identify and quantify the different types of traps existing in the semiconductor device. This measurement technique utilizes the time domain analysis to investigate the time evolution of charge carriers associated with the trapping and de-trapping process. Detailed explanations of the measurement technique can be found in [3.36], [3.50], [3.51]. The principle of this measurement technique involves that the device is initially biased in traps-filling condition (capture process: $V_{GS,F}$, $V_{DS,F}$) for fixed period of time, 1 ms, then the bias is changed to de-trapping condition (emission process: $V_{GS,M}$, $V_{DS,M}$), thus inducing both the trapping and de-trapping process. The filling pulse can be applied either on the gate or drain or on both sides of the device terminals, the corresponding drain current characteristics measured allows to identify the existence of different traps. The recovering of drain current (I_D) due to the emission of trapped charges is measured over several time decades by using the sampling digital oscilloscope with multi-recording technique. The measurement process can be repeated at different temperatures by applying the same filling pulses to the device. Since the emission of traps is thermally activated, the emission time constant of traps changes with temperature. By using the Arrhenius equation, the physical properties of traps such as the apparent activation energy (E_a) and cross section (σ_n) can be extracted.

Fig. 3.30 shows the DCTS measurement result of the 6×75 µm GaN/AlGaN/GaN HEMT on SiC substrate. The gate bias-voltage (V_{GS}) of the device is fixed at -3.1 V (close to device pinch-off) and the drain voltage (V_{DS}) is pulsed from 9 V to 19 V and is maintained at 19 V for 1 ms (pulse width = 1 ms) and then, it is changed again to 9 V. This biasing conditions corresponds to deep class-AB operation mode, which is widely used for designing RF power amplifiers. The corresponding recovering of drain current due to emission of traps is measured for 19 ms (pulse period = 19 ms) using the sampling oscilloscope. When the drain bias voltage is changed from 19 V to 9 V, a transient drain current recovery related to the emission of traps is observed. The measured transient drain current characteristics with a relative long time constant, for recovery of drain current confirms the existence of traps in the device. However, it is important to identify the location of traps in the device. The traps could be located either at the surface or barrier or bulk of the device. In order to identify the exact location of these traps, two-dimensional TCAD

physical simulations have been carried out for this device. The obtained simulation results are explained in the next section.

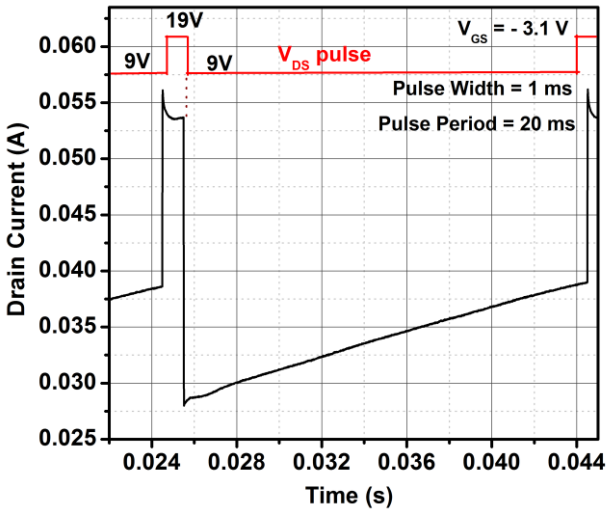


Fig. 3.30. 6×75 µm Drain lag transient measurement using DCTS method.

3.8.2. Intepretation Based on TCAD Physical Simulations

Two-dimensional physical simulations have been carried out by using the schematic structure shown in Fig. 3.9 (a). The polarization charges described in section 3.6.2 have been used in our simulations. Moreover, the surface donors are introduced at the GaN cap layer/SiN interface in order to form the 2DEG in the GaN channel. Donor-like traps with a density of 1.0×10^{13} cm^{-2}, having an energy level of 0.2 eV below the conduction band are used. In addition, acceptor-like traps, having an energy levels of 0.51 and 0.57 eV are introduced in the GaN buffer and the assumed density of both traps is 5.0×10^{16} cm^{-3}, respectively. Electron and hole capture cross sections of both these traps are assumed to be 5.0×10^{-16} and 1.0×10^{-20} cm^2, respectively. In the AlGaN barrier region, acceptor-like traps, having a concentration of 5.0×10^{16} cm^{-3} and at the specified energy level of 0.5 eV are introduced. Electron and hole capture cross sections of barrier traps are assumed to be 1.0×10^{-18} and 1.0×10^{-20} cm^2, respectively. Fig. 3.31 (a) and (b) shows the dc-IV and transient simulation characteristics of the device at 25ºC, by considering the different cases of traps in the device structure. For transient simulation, the gate voltage (V_{GS}) of the device is biased at -3.1 V (close to device pinch-off) and the drain voltage (V_{DS}) is pulsed from 0 V to 19 V and is maintained at 19 V for 1 ms (pulse width = 1 ms) and then, it is changed to 9 V. Then, the recovery of drain current due to emission of traps has been simulated for time decades varying from 2 ms to 1 s. From the Fig. 3.31 (b) it is clear that the

traps introduced in the AlGaN barrier have no influence on the simulated transient characteristics.

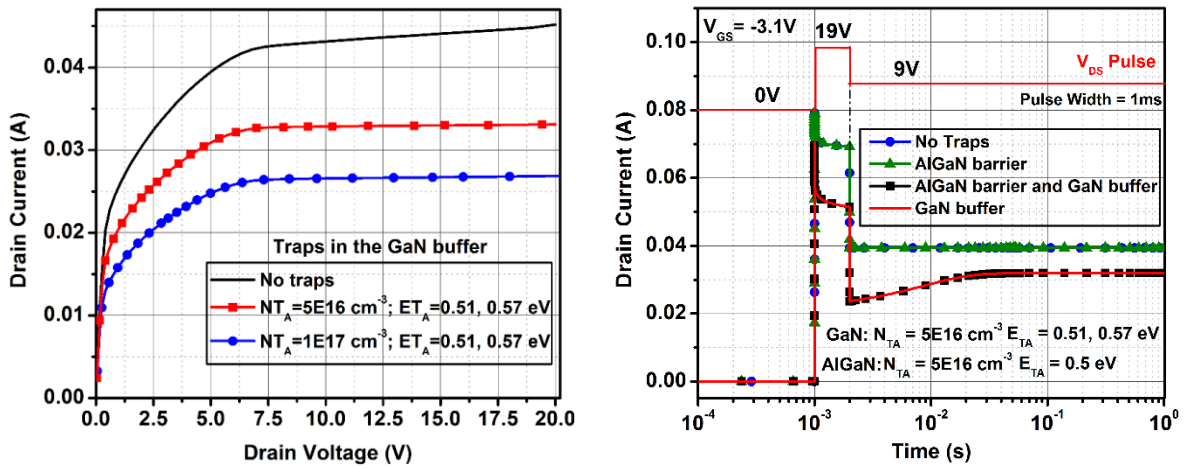
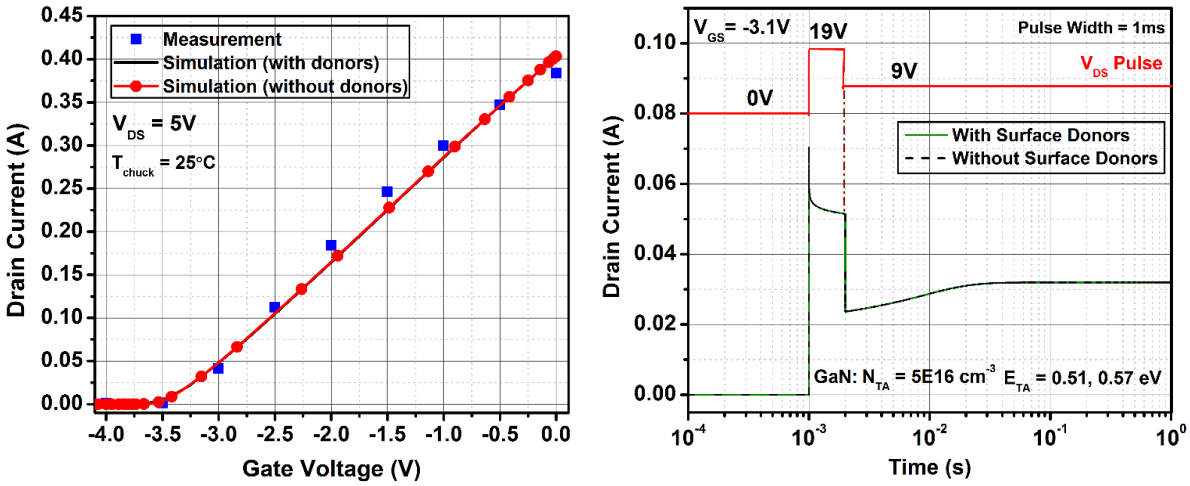


Fig. 3.31. (a) Simulated dc-IV drain current characteristics of 6×75 µm device, by considering the different concentration of traps in the device structure (b) transient drain current characteristics by considering the different cases of traps. Blue line with round symbol indicates there are no traps in the device. Green line with triangle symbol shows the case of traps existing only in the AlGaN barrier. Black line with square symbol shows the transient characteristics with traps existing in both the AlGaN barrier and GaN buffer. Red line shows the case of traps only in the GaN buffer. Surface donors exist in all the aforementioned cases.

This demonstrates that if the traps exist in the AlGaN barrier and if the drain voltage is pulsed from one bias to another (drain-lag measurement), it may not affect the measurement characteristics. However, if the gate voltage is pulsed, it will have significant influence on the transient characteristics (section 3.9). Therefore, the transient behavior observed in measurement can be reproduced by simulations providing that donor-like and acceptor-like traps are placed at the surface and in the GaN buffer. Hence, the traps are either located in the GaN buffer or at the surface. In order to further identify the location of the traps in the device, the surface traps have been replaced with an equivalent fixed charge, whose concentration is assumed to be 0.8×10^{13} cm^{-2}, respectively. This particular value is assumed because, this does not affect the calibrated TCAD simulation model and reproduces the experimentally measured I-V characteristics. Fig 3.32 (a) and 3.32 (b) show the simulated dc and transient drain current characteristics of the device, with and without the surface donors defined in the device. The same simulation characteristics have been obtained for both cases (with and without surface donors) and hence, the GaN buffer traps are responsible for the decrease in current characteristics observed in measurement.



(a) (b)

Fig. 3.32. Simulated dc (a) and transient (b) drain current characteristics of 6×75 µm device, with and without the surface donors. Buffer traps exist in both cases and it is confirmed that slow transient observed is due to GaN buffer traps.

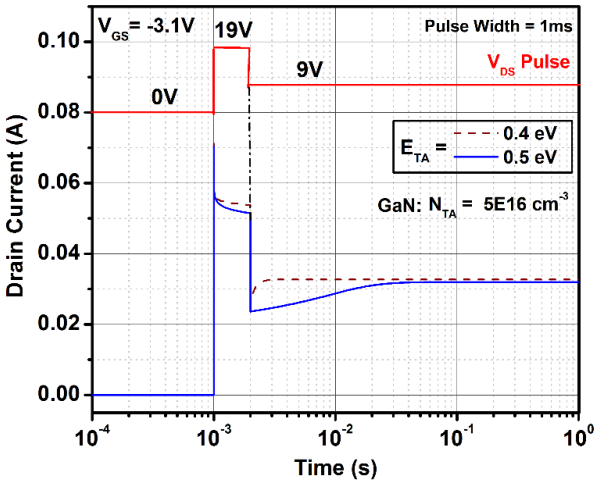
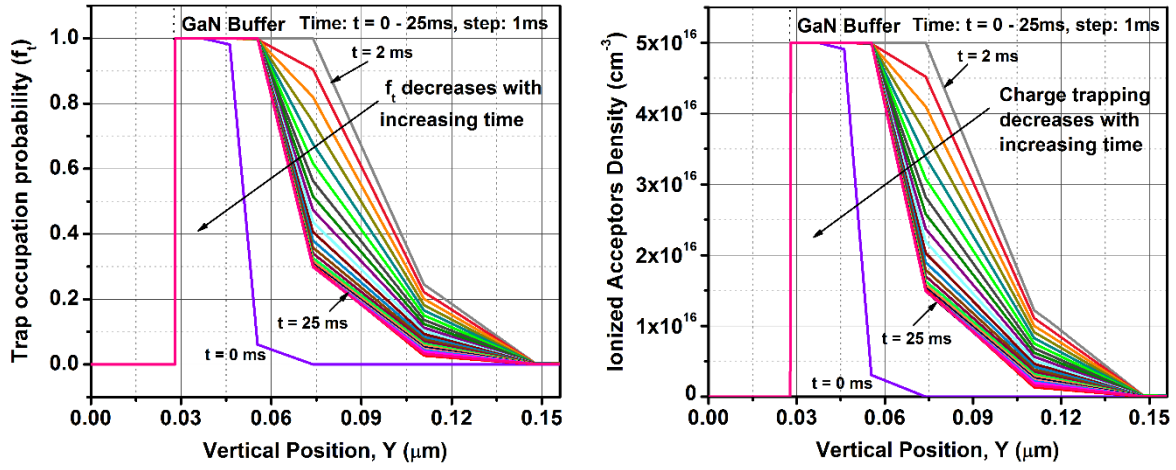


Fig. 3.33. Simulated transient drain current characteristics of 6×75 µm device. Deeper the level of buffer traps, larger the time required to attain the steady state drain current.

Fig. 3.33 shows the transient simulation characteristics of the device by considering one trap level in the GaN buffer region and with two different energy levels. The trap concentration is assumed to be 5.0×10^{16} cm^{-3}, respectively. The simulation result demonstrates that buffer traps with an energy level of 0.4 eV has the smaller emission time constant compared to 0.5 eV. Therefore, deeper the trap energy level, more the possibility of ionization of acceptor traps, larger the time required to attain the steady state drain current.

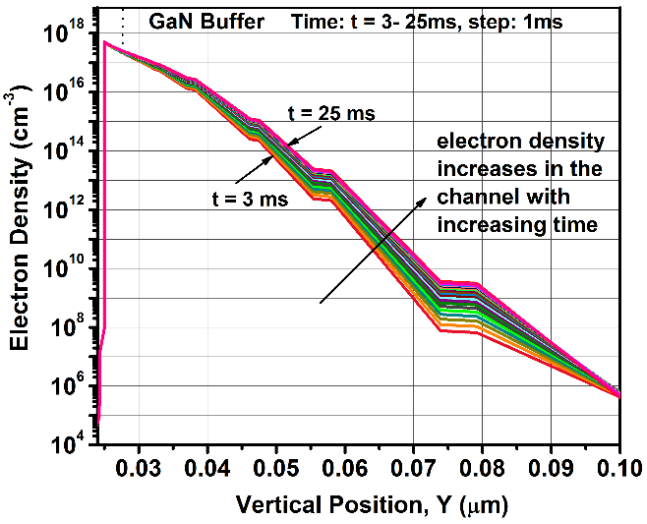
In order to understand the physics behind the initial decrease and the recovery of drain current as a function of time, a detailed analysis showing the time evolution of the electron density and

trapped charge distributions during the drain current transients have been performed. Fig. 3.34 (a) and (b) show the probability of trap occupation and ionized trap density as a function of device position inside the GaN buffer (vertical cut is made at X = 1.1 µm, drain-side gate edge) and for different transient times. It can be seen that the trap occupation probability and the density of ionized traps inside the GaN buffer region decreases with increasing time. This is because the traps slowly begin to emit the electrons and hence the drain current slowly recovers to the steady state current value. A vertical cut (under the gate) and horizontal cut (along the AlGaN barrier/GaN channel interface, where the 2DEG sheet density is high) are made on the device and the respective electron density as a function of device distance is shown in Fig. 3.35 (a) and (b), respectively.

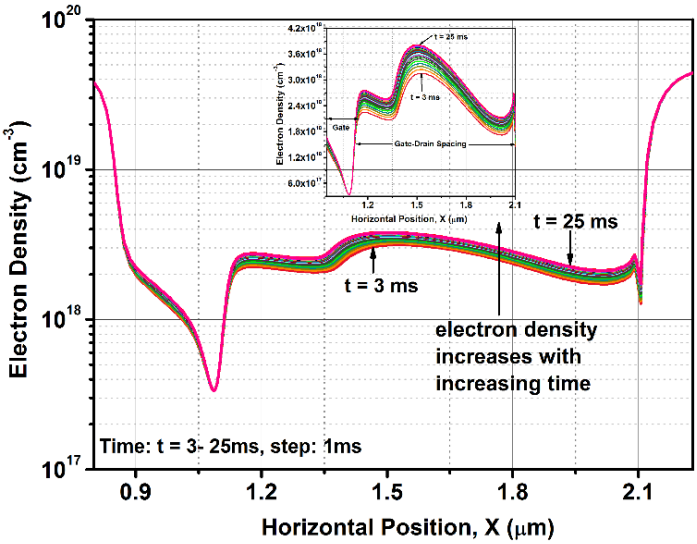


(a) (b)

Fig. 3.34. Simulated trap occupation probability (a) and ionized-trap density (b) distribution through the GaN buffer layer at different times for E_{TA} = 0.5 eV case shown in Fig. 3.33.



(a)



(b)

Fig. 3.35. Simulated electron density as a function of vertical (a) and horizontal device distance (b) at different times for the E_{TA} = 0.5 eV case shown in Fig. 3.33.

The inset plot in Fig. 3.35 (b) shows the zoomed view of the gate and gate-drain access regions. It can be observed, as the time increases, the electron density in the channel increases which indicates that the trapped charges are released back into the channel and hence, increasing the simulated electron density and thereby increasing the drain current. Therefore, this simulation study confirms that traps in the GaN buffer are responsible for the decrease in drain current (drain lag phenomenon) observed in the drain-side excited DCTS measurement. Moreover, deeper the activation energy level of traps in the bandgap, larger the time required to attain the steady state drain current. Further, larger the magnitude of drain voltage may be required to excite the traps.

3.9. Gate – Lag TCAD Simulation Study

In the section 3.6.5, traps in the AlGaN barrier cannot be identified using low-frequency admittance measurements. However, they can be identified using gate-lag transient measurement. In this section, the impact of AlGaN barrier traps on the transient drain current characteristics have been investigated using TCAD physical simulations. Fig. 3.36 shows the schematic structure of the device used for performing gate lag simulations. The 22-nm AlGaN barrier layer is divided into three sub-layers namely AlGaN top, AlGaN middle and the AlGaN bottom. The thickness of the AlGaN top and bottom layers are 4-nm each, whereas the thickness of the AlGaN middle layer is 14-nm, respectively. Donor-like traps are introduced in the AlGaN top at the specified energy level of 0.3 eV below the conduction band. Similarly, acceptor-like

traps are placed at the AlGaN bottom region which is close to the GaN channel. The trap concentration is N_{TA} = 1.0× 10^{17} cm^{-3} and both the electron and hole capture cross sections of traps are assumed to be 1.0× 10^{-15} cm^2, respectively.

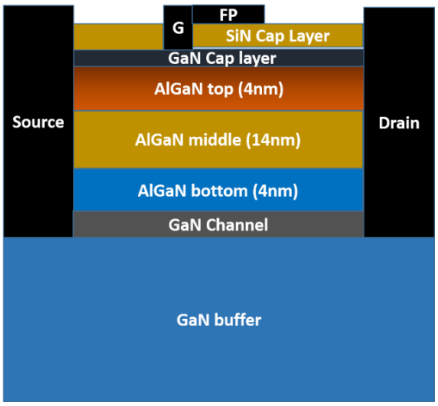
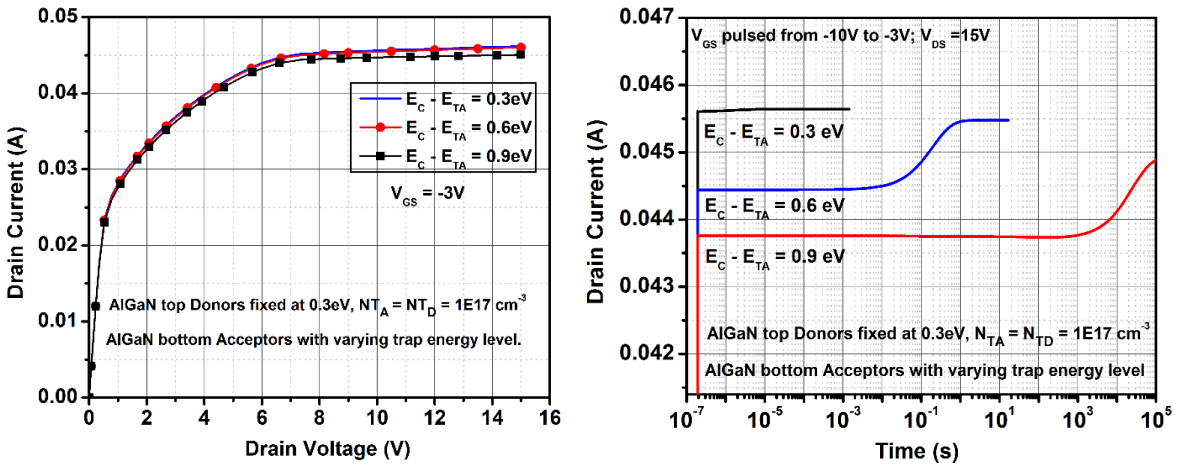


Fig. 3.36. Schematic of the GaN/AlGaN/GaN HEMT used for transient gate lag simulations.

Traps energy level (E_{TA}) is considered as a varying parameter in order to study the influence of energy level of traps on the simulated transient characteristics. Fig. 3.37 (a) and Fig. 3.37 (b) show the simulated dc-IV and transient drain current characteristics of the device for varying acceptor-like traps energy level.



(a) (b)

Fig. 3.37. Simulated dc-IV (a) and gate-lag transient (b) characteristics of 6×75 µm device with both acceptor and donor-like traps in the GaN buffer. Deeper the energy level of acceptor-like traps, longer the time required to attain the steady state drain current.

The simulated characteristics indicates that the traps introduced in the AlGaN barrier capture electrons from the channel and therefore the drain current remains at a lower value for some period of time until the traps start to re-emit the captured electrons back into the channel region.

Moreover, the deeper the energy level of acceptor-like traps, greater the possibility of ionization of acceptors and the longer the time required to reach the steady state drain current. The donor-like traps have less influence (verified using several simulations) on the simulated transient characteristics as they are located far away from the channel. This result suggests that traps in the AlGaN barrier can be identified using gate-lag measurements.

3.10. Summary

In this chapter, the activation energy and cross section of the traps present in the GaN buffer of the GaN/AlGaN/GaN HEMT device has been extracted using LF S-parameter and noise measurements. Moreover, the TCAD physical simulation results of the device have been presented. The TCAD physical models and calibration procedure have been described in detail. Using the calibrated TCAD device model, LF admittance simulations have been performed. Good agreement has been achieved between the simulated and measured Y_{22} parameter. This strongly suggests that LF admittance measurement is an effective tool for characterizing GaN buffer traps. Similarly, using the noise simulation results, it has been confirmed that traps exist in the GaN buffer of the device. Good agreement has been achieved between the simulated and measured output drain noise spectral density for device temperatures between 25ºC and 100ºC. The simulation results demonstrate that LF noise measurement is an effective tool for identifying the traps present in the GaN buffer. Time-domain drain lag measurements have been carried out using the DCTS measurement technique. Traps in the GaN buffer cause the short-term reduction in drain current when the drain bias is varied, and as the time increases, the drain current recovers slowly to the steady state drain current. The TCAD simulation results reveal that traps in the GaN buffer are responsible for this observed drain-lag phenomenon. The simulation results also reveal that traps in the AlGaN barrier cannot be identified using LF measurements. It could be possible through gate-lag measurements. Therefore, the simulation results presented in this chapter establish a correlation with measurements in order to identify the location of traps in devices and this could provide an efficient feedback mechanism for improving the GaN HEMT technology and thereby its RF performances.

Acknowledgement

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Chapter 4

Characterization of AlN/GaN/AlGaN HEMTs grown on Si and SiC Substrate through On-Wafer Measurements and TCAD-based Physical Device Simulations

Based on Publications:

1. **N. K. Subramani**, A. K. Sahoo, J-C. Nallatamby, R. Sommet and R. Quéré, "Systematic Study of Traps in AlN/GaN/AlGaN HEMTs on SiC Substrate by Numerical TCAD Simulation", *12th Conference on PhD Research in Microelectronics and Electronics (PRIME)*, pp: 1 – 4, June. 2016.

2. A. K. Sahoo, **N. K. Subramani**, J-C. Nallatamby, N. Rolland, R. Quéré and F. Medjdoub, "Temperature Dependent Contact and Channel Sheet Resistance Extraction of GaN HEMT", *Integrated Nonlinear Microwave and Millimeter-wave Circuits Workshop (INMMIC)*, pp: 1 – 3, Oct. 2015.

3. **Nandha Kumar Subramani**, Amit Kumar Sahoo, Jean-Christophe Nallatamby, Raphael Sommet, Nathalie Rolland, Farid Medjdoub and Raymond Quéré, "Characterization of Parasitic Resistances of AlN/GaN/AlGaN HEMTs through TCAD-Based Device Simulations and On-Wafer Measurements", *IEEE Trans. on Microwave Theory and Techniques*, vol. 64, pp: 1351 – 1358, May 2016.

Chapter 4. Characterization of AlN/GaN/AlGaN HEMTs grown on Si and SiC Substrate through On-wafer Measurements and TCAD-based Physical Device Simulations

4.1. Systematic Study of Traps in AlN/GaN HEMTs using Numerical Simulation

4.1.1. Introduction

The limitations of conventional semiconductors for RF and microwave power applications have paved the way for wide-band gap group III –V materials such as GaN, SiC etc. Among these, GaN material receives much attention due to its superior material properties [4.1] such as high electron mobility, high saturation velocity and high breakdown electric field. AlGaN/GaN High Electron Mobility Transistors (HEMTs) have proven to be an excellent candidate for high power microwave and mm-wave applications [4.2]. Moreover, in recent years, the demand for high frequency performance of AlGaN/GaN HEMT devices are steadily increasing [4.3]. In order to extend the frequency of operation of these devices, it is necessary to implement ultra-short gate lengths and using of thin AlGaN barrier [4.4]. However, reducing the thickness of AlGaN barrier below a certain limit (about 10 nm) results in a strong degradation of the two-dimensional electron gas density (2DEG), and thus poor device performance [4.5]. Although increasing the Al content in the AlGaN barrier layer can improve the 2DEG density, it also increases the lattice mismatch between the AlGaN and GaN layers, thereby degrading the quality of the heterostructure [4.6]. Furthermore, implementing the gate recess technique on these devices is difficult and this generally induces high gate leakage and reliability problems [4.5]. In recent years, AlN/GaN HEMT technology has become popular owing to its high theoretical 2DEG density of 6×10^{13} cm^{-2} [4.7]. This is due to the high spontaneous polarization value of AlN material [4.8] and its wide-band gap of 6.2 eV compared to GaN (3.42 eV). It has been demonstrated [4.9] that the replacement of the conventional AlGaN barrier layer by AlN/GaN layers offers much higher 2DEG density, allowing the achievement of high drain current (~2A/mm), even using ultrathin AlN barrier layer thickness well below 10 nm. Furthermore, the AlN/GaN HEMT devices achieve high breakdown voltages and lower on-resistance [4.10]. This could be a suitable alternative to replace the existing conventional AlGaN/GaN HEMT technology for high frequency applications.

Although this AlN/GaN HEMT technology has made substantial progress over the last few years [4.11], the performance is still limited by the presence of electronic traps in the device structure. The traps may present at the surface, bulk or at the interface, causing effects such as current collapse, transconductance frequency dispersion, gate lag and drain lag.

Moreover, only a very limited number of publications are available to describe the influence of traps in these device structures. Therefore, the analysis of trapping effects on the device performance is significantly important in order to provide an appropriate feedback for the future technological improvements.

In this first section of this chapter, we study the impact of GaN channel traps on the performance of AlN/GaN/AlGaN HEMT using two-dimensional TCAD Sentaurus physical device simulation. Traps specifications used for TCAD simulations are adopted from the data reported in the literature [4.12]. In the second section of this chapter, we investigate the temperature dependency of on-resistance of AlN/GaN/AlGaN HEMT devices grown on SiC substrate through dc and low-frequency S-parameter measurements. A simple methodology to extract the temperature and bias dependent channel sheet resistance and parasitic contact resistance of GaN HEMT technology have been proposed.

4.1.2. Experimental and Numerical Device Simulation Structure

The AlN/GaN/AlGaN heterostructure field-effect transistors (HFETs) were grown by metal-organic chemical vapor deposition (MOCVD) on a 380-µm SiC substrate. The epilayers consist of a 1.5-µm thick $Al_{0.08}Ga_{0.92}N$ buffer layer, 150-nm thick GaN channel layer followed by a 6-nm ultrathin AlN barrier layer and 3-nm in-situ grown Si_3N_4 cap layer. Ni/Au Schottky gate contact and Ti/Al/Mo/Au metal stack for ohmic source and drain contacts were deposited directly on top of the AlN barrier layer by etching the in-situ Si_3N_4 layer. The in-situ Si_3N_4 layer allows for handling strain relaxation resulting from the high tensile stress induced in the device structure because of the growth of AlN barrier layer on top of the GaN channel layer and thereby giving rise to a high surface quality [4.5].

The devices with different gate widths, W_G of 25 µm, 50 µm and 100 µm, each with two fingers (n=2) were fabricated on the same wafer. The gate length L_G of the devices is 0.2 µm, source-gate separation (L_{SG}) were fixed to 0.4 µm and different gate-drain distances (L_{GD}) of 1, 2 and 3 µm, respectively, were used for the fabrication of devices. Room temperature dc-IV characteristics of the fabricated device are measured using an Agilent B1500A semiconductor device parameter analyzer. The cross section of the structure used for the simulation is shown in Fig. 4.1. The nominal thickness of all layers are used except for the case of SiC substrate. The SiC substrate thickness is considered to be 5 µm, in order to speed up the simulation time. Moreover, it is determined in the simulation that any further increase in thickness of the SiC substrate after 5-µm will have no significant effect on the simulated dc-IV characteristics.

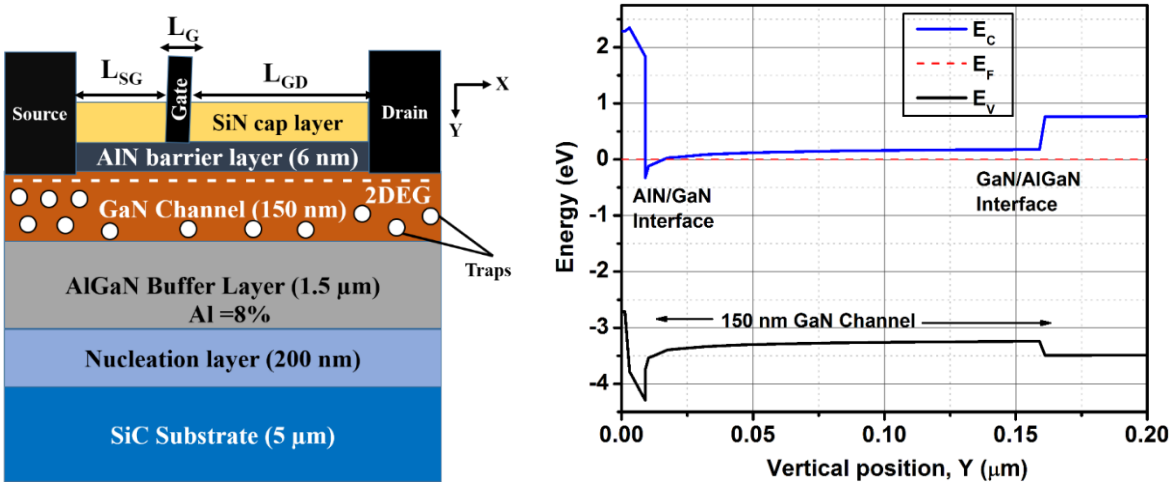


Fig. 4.1. (a) Cross section of an AlN/GaN/AlGaN HEMT used for simulation (b) Simulated energy band diagram under equilibrium condition.

4.1.3. Numerical TCAD Device Simulations

Two-dimensional physics based numerical simulations have been carried out using the commercially available TCAD Sentaurus software (formerly ISE-DESSIS) from Synopsys Inc. Poisson's equation, and continuity equations for both electrons and holes, and the drift-diffusion (DD) model transport equations are solved self-consistently. The electric field induced due to the piezoelectric and spontaneous polarization contributes to the formation of 2DEG density at the AlN/GaN heterojunction interface, even without the need for doping [4.8]. In absence of externally applied electric fields, the polarization charges formed are of course, equal in magnitude and opposite in sign to maintain the overall charge neutrality of the device [4.13]. The theoretical method used for the calculation of polarization charges was described in [4.8]. However, in the case of AlN/GaN HEMT heterostructure, the theoretically calculated polarization charges are slightly higher than the experimentally measured sheet carrier concentration. A positive fixed sheet charge ($+\sigma_{pol}$) having a density 2.0×10^{13} cm^{-2} is defined at the AlN/GaN interface, which is in agreement with the experimental value [4.10]. The equivalent negative charge ($-\sigma_{pol}$) having the same density is placed at the AlN/SiN interface. According to surface donor theory [4.14], the surface donors are responsible for the 2DEG channel formation in GaN HEMT devices. Hence, donor-like traps (σ_{TD}) having a density of 3.5×10^{13} cm^{-2}, with an energy level of 0.2 eV above the mid bandgap are introduced at the AlN/SiN interface. Electron (σ_n) and hole (σ_p) capture cross sections are assumed to be $\sigma_n = \sigma_p = 1.0\times 10^{-15}$ cm^2, respectively. For the simulation, constant mobility and field dependent

mobility models are included for electrons and holes and Shockley-Read-Hall recombination model is used for carrier generation and recombination. The summary of the material parameters used in the simulations are listed in Table 4.1. The energy band diagram of the simulated structure under equilibrium condition is shown in Fig. 4.1 (b).

In order to analyze the device characteristics, the simulation model needs to be properly calibrated to ensure that the simulated characteristics are in agreement with the experimentally measured characteristics. The calibration process initiates with fitting the pinch-off in simulation to experiment by adjusting the Schottky gate work function (4.25 eV). Then, by using the low field mobility and saturation velocity parameters of GaN material, the linear and saturation region drain current characteristics are calibrated. More details about the TCAD simulation model calibration process is given in Chapter 3 (section 3.6.1 – 3.6.3). Fig. 4.2 (a) shows the comparison of the simulated and measured transfer and transconductance characteristics of the 2×100 µm device at drain-source bias voltage, V_{DS} = 5 V and temperature, T = 25ºC. Fig. 4.2 (b) shows the simulated and experimental dc-output characteristics for gate-source bias voltage, V_{GS} values varying from -2.5 V to 0.0 V in steps of 0.5 V. A good agreement between the simulation results and experimental data confirms the validity of the calibrated physical model. It is worthwhile to note that no traps are used in the device structure while performing the calibration of the simulation model. This will allow us to analyze the impact of different traps on device performances.

Table 4.1. Summary of the material parameters used in TCAD simulations.

Material Property	**Units**	**GaN**	**AlN**
Electron Mobility	$cm^2/V\ s$	1000	300
Bandgap	eV	3.42	6.12
Relative permittivity	-	9.5	8.5
Electron affinity	eV	4.0	1.84
Electron saturation velocity	cm/s	9.0×10^6	1.5×10^7
Effective conduction band density of states	cm^{-3}	2.24×10^{18}	4.1×10^{18}
Effective valence band density of states	cm^{-3}	2.51×10^{19}	2.84×10^{20}

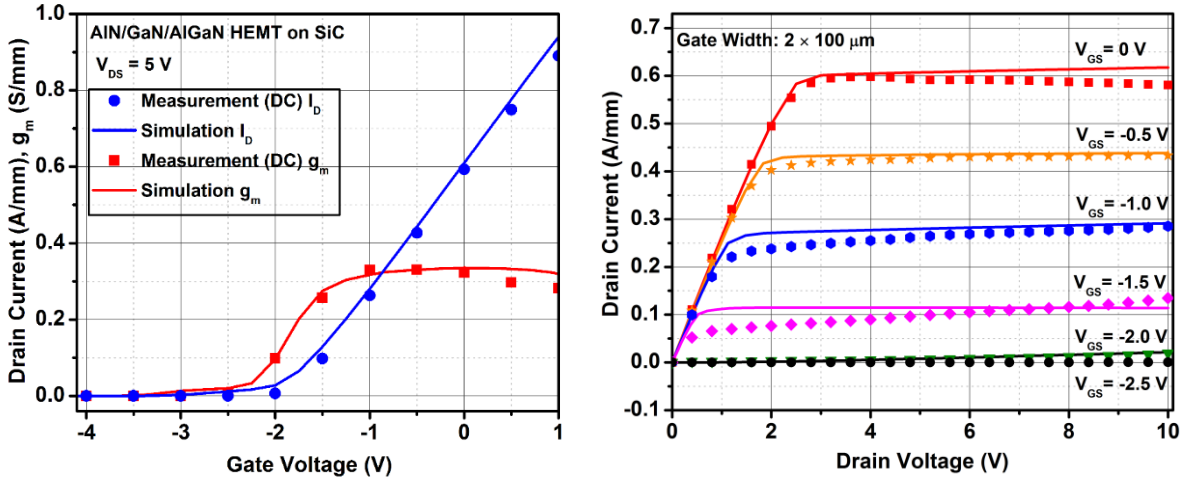
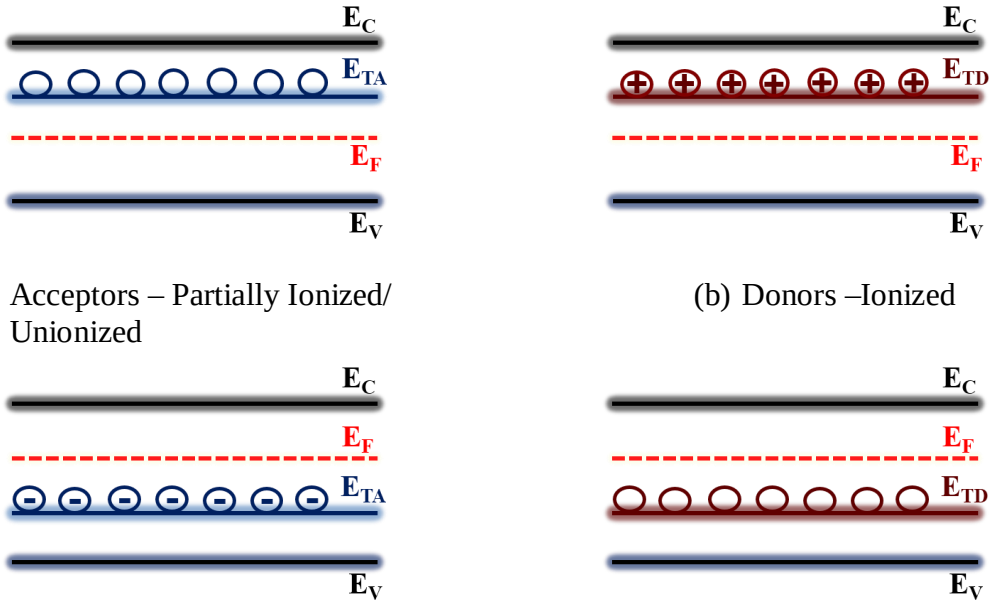


Fig. 4.2. Comparison of 2×100 µm AlN/GaN HEMT device measurement (symbols) and simulation (solid lines) results: transfer and transconductance characteristics at V_{DS} = 5 V (a) and output characteristics for varying V_{GS} between 0 V and -2.5 V in steps of 0.5 V.

4.1.4. Impact of Traps on Simulated dc-IV Characteristics

Traps can be categorized into two types: donor-like and acceptor-like traps. An acceptor-like trap is considered to be neutral, if empty (unionized) and negative, if occupied (ionized), whereas a donor-like trap is positive, if empty and neutral, if filled with an electron. The ionization or non-ionization of traps inside the device depends strongly on the location of its energy level (E_T) with reference to Fermi-energy level (E_F).



(a) Acceptors – Partially Ionized/ Unionized

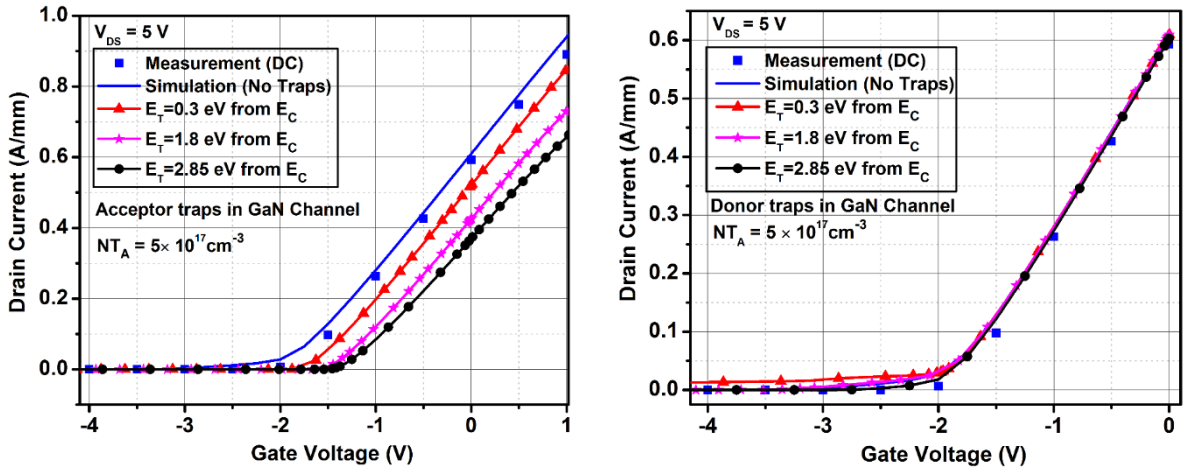
(b) Donors –Ionized

(c) Acceptors – Ionized

(d) Donors –Unionized

Fig. 4.3. Impact of type of traps and its associated energy level in the energy band diagram.

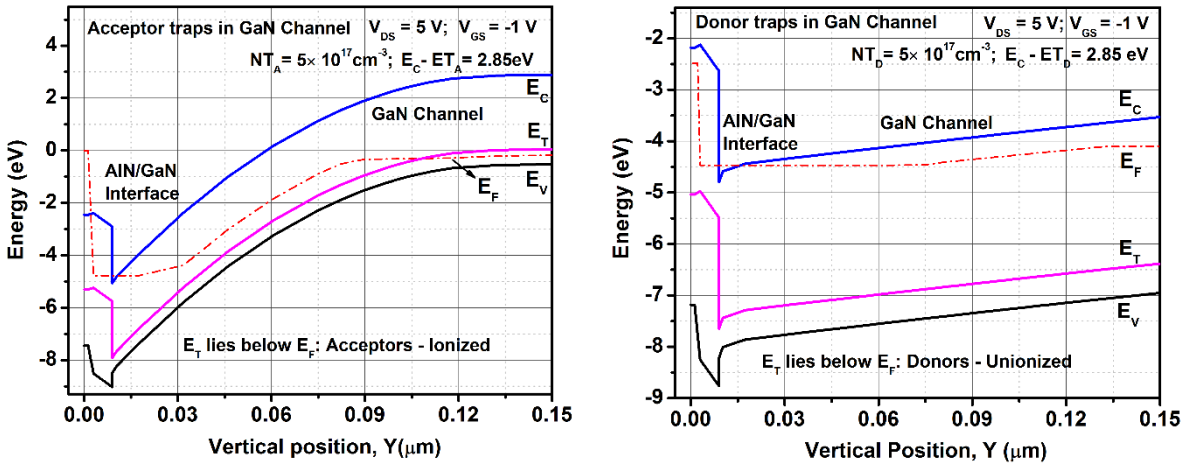
For instance, if the acceptor-like traps energy level (E_{TA}) is located well above the E_F, the traps remain unionized and if E_{TA} is below the E_F, all the traps get ionized. Fig. 4.3 shows the influence of acceptor and donor-like traps on the energy band of the material or device under equilibrium condition. In order to analyze the impact of these traps, acceptor-like traps are introduced in the GaN channel, whose trap energy level (E_{TA}) and trap concentration (N_{TA}) are considered as a varying parameter. Fig 4.4 (a) shows the influence of acceptor traps, having a different trap energy level on the simulated dc-IV characteristics of the 2×100 µm device. It can be seen that acceptor traps whose energy level lies deep inside the conduction band causes a significant drain current decrease and also the shift of pinch-off voltage. The donor-like traps are introduced in the GaN channel similar to the trap energy levels shown in Fig. 4.4 (a), the donor traps get ionized only for a very high negative gate bias values and for the energy levels close to the conduction band. Fig. 4.4 (b) shows the simulated dc-IV characteristics with varying donor energy levels inside the GaN channel. In the dc-IV simulation, donor-like traps are ionized only when the specified energy level is above the E_F and acceptor-like traps are ionized only for the energy levels under E_F as illustrated in Fig. 4.3.



(a) (b)

Fig. 4.4. Influence of acceptor traps in the GaN channel on the simulated transfer characteristics for NT_A = 5.0 ×10^{17} cm^{-3} and for various trap energy levels.

Fig. 4.5 (a) and 4.5 (b) show the energy band diagram of the device with either acceptor or donor traps present in the GaN channel (a vertical cut is made in the gate-drain region, X = 1.35 µm, close to the gate end), whose trap energy level is 2.85 eV below the conduction band and the assumed trap concentration is 5.0× 10^{17} cm^{-3}. The trap energy level (E_T) lies well below E_F for both cases under the biasing conditions of V_{DS} = 5V and V_{GS} = -1 V.



(a) (b)

Fig. 4.5. Simulated energy band diagram of the device by considering acceptor (a) and donor (b) traps in the GaN channel whose trap energy level is 2.85 eV below the conduction band. Acceptor traps ionizes only when E_T is below E_F and donor traps ionizes for E_T above E_F.

This will cause ionization of all acceptor traps in the GaN channel and thereby degrade the drain current, whereas the donor traps remain unionized. Fig 4.6 shows the energy band diagram of the device with donor traps, having an energy level of 0.3 eV below the conduction band and for the biasing conditions of V_{DS} = 5V and V_{GS} = -4 V. It can be seen that E_T lies above E_F, causing ionization of donor traps introduced in the GaN channel of the device. Therefore, it can be concluded that donor traps will ionize only at high negative gate biases and only when the trap energy level is shallow inside the bandgap and thus, donor traps have no significant influence on the simulated dc-IV characteristics.

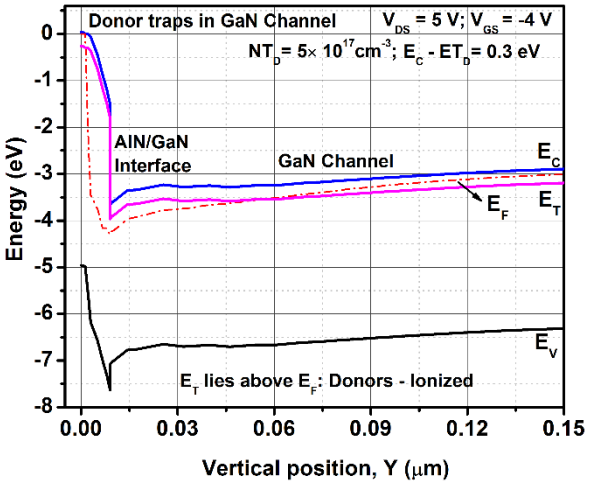


Fig. 4.6. Simulated energy band diagram of the device by considering donor traps in the GaN channel whose trap energy level is 0.3 eV below the conduction band. Biasing conditions: V_{DS} = 5V and V_{GS} = -4 V.

Fig. 4.7 shows the probability of traps occupation as a function of device distance inside the GaN channel and for various E_{TA}. It is evident that deeper the energy level of acceptor traps, larger the region of ionization of traps inside the GaN channel and thereby larger the reduction in drain current.

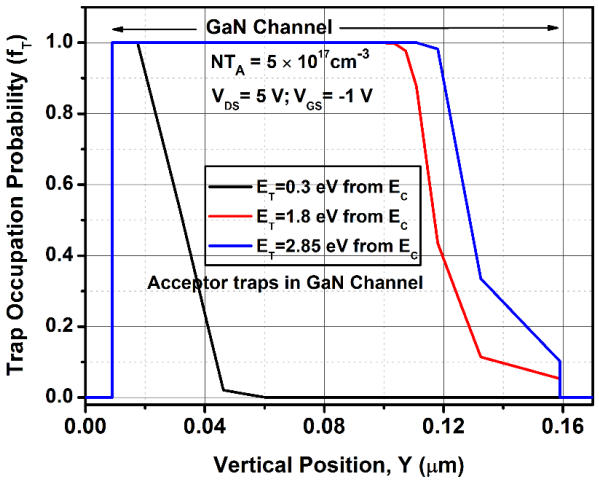
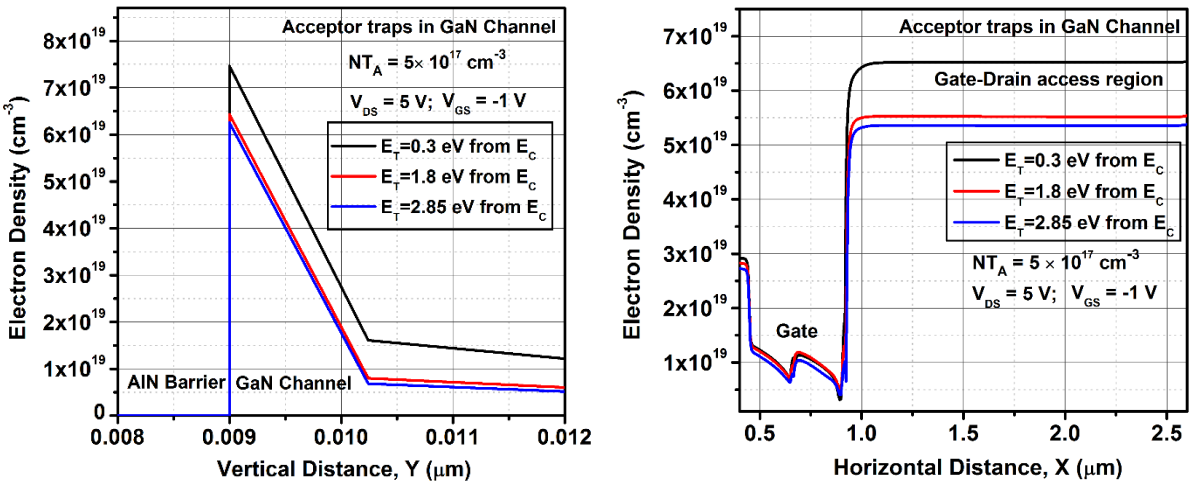


Fig. 4.7. Simulated traps occupation probability by including acceptor traps in the GaN channel. Biasing conditions: V_{DS} = 5V and V_{GS} = -1 V.



(a) (b)

Fig. 4.8. Simulated electron density in the channel as a function of vertical (a) and horizontal (b) device distance, for various acceptor traps energy level. Biasing conditions: V_{DS} = 5V and V_{GS} = -1 V.

Fig. 4.8 (a) and 4.8 (b) show the electron density in the channel region as a function of horizontal (cut is made along the AlN/GaN interface) and vertical (cut is made in the gate-drain region, close to the gate end) device distance, for various acceptor traps energy level. As expected, deeper the trap energy level, larger the ionization of acceptors, larger the reduction of electrons in the channel.

Fig. 4.9 shows the electron density in the channel region as a function of horizontal (cut is made along the AlN/GaN interface) device distance and for various donor traps energy level. The donor traps remains unionized for the biasing conditions of V_{DS} = 5V and V_{GS} = -1 V and hence, the electron density in the channel remains the same, irrespective of the introduced donors.

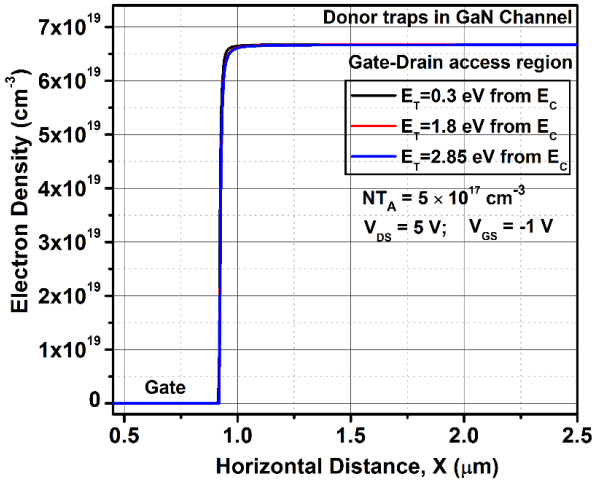


Fig. 4.9. Simulated electron density in the channel as a function of horizontal device distance and for various donor traps energy level. Biasing conditions: V_{DS} = 5V and V_{GS} = -1 V.

4.2. Characterization of Parasitic Resistances of AlN/GaN HEMTs Grown on SiC Substrate

4.2.1. Introduction

Although AlN/GaN HEMTs have demonstrated their superior potential for high power microwave and mm-wave applications. Obtaining a very low on-resistance (R_{ON}) immediately after switching from a high-voltage OFF state to a low-voltage ON state is a critical requirement in power electronics applications [4.15]. The higher electron mobility in the two-dimensional quantum well presents a low R_{ON} value that enhances the RF power-added efficiency performance [4.16]. In RF power GaN HEMT devices, dynamic switching issues occur due to current collapse, gate lag and drain lag effects, which deteriorates the RF power performance [4.17]. In power switching applications, this issue is visible, where the R_{ON} remains high for a period of time after an OFF-ON switching event [4.18]. In addition, the temperature has a significant impact on R_{ON}. The reduction of the 2DEG mobility with the increase of temperature contributes to the increase of R_{ON} [4.19]. Moreover, a power switching transistor usually operates at a relatively high temperature. Therefore, the analysis of the temperature dependent R_{ON} is an active research topic to explore. There are numerous papers reported in literature [4.19]–[4.24] for the temperature dependent characterization of AlGaN/GaN HEMT

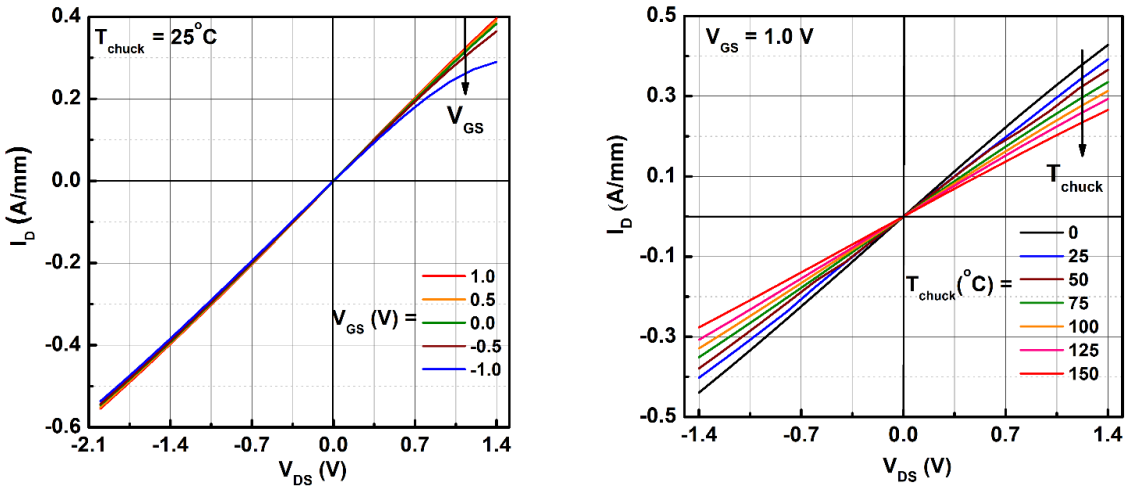
technology. However, as this AlN/GaN/AlGaN HEMT technology is relatively new, there has been little research on this device technology [4.25], [4.26]. The aim of this section of the chapter, is to contribute to the temperature dependent R_{ON} extraction [4.27] of AlN/GaN/AlGaN HEMT technology using on-wafer measurements and TCAD based device simulations. Additionally by applying a simple technique, to extract the temperature and bias dependent channel sheet resistance (R_{sh}) and parasitic series contact resistance (R_{se}) of this technology. The proposed method could be applied to any device technology in order to extract the channel sheet resistance and parasitic contact resistances. In this paper, we attempt to study only the static R_{ON} of the device. The drain bias voltage used for the measurements is very low which implies that there is no visible trapping effect. However, under high biasing and high-temperature operating conditions, the presence of electronic traps in the device structure gets activated and contributes to dynamic R_{ON}. Therefore it is useful to analyze the impact of dynamic R_{ON} on device performance due to traps [4.15], [4.28], [4.29]. Moreover, the accurate modeling of trapping effects can significantly improve the performance of large signal model (LSM) and this is particularly important for designing high power RF amplifiers [4.30]–[4.32].

4.2.2. DC Measurements

On-wafer DC-IV measurements are performed for different geometries of AlN/GaN/AlGaN HEMTs grown on SiC substrate. The measurements have been carried out at different chuck temperatures (T_{chuck}) between 0ºC and 150ºC using an Agilent B1500A semiconductor device parameter analyzer (SDA). Fig. 4.10 (a) and 4.10 (b) show the measured DC-IV output characteristics of the 2×100 µm device with L_G =0.2 µm, L_{SG} =0.4 µm and L_{GD} = 2 µm. The output characteristics are shown for different V_{GS} between 1.0 V and -1.0 V for a chuck temperature (T_{chuck}) of 25ºC and for various T_{chuck} between 0ºC and 150ºC at V_{GS} =1.0 V, respectively. The derivatives are calculated from the measured I_D-V_{DS} curve at the point where the gate-source voltage, V_{GS} equals drain-source voltage, V_{DS}. The corresponding R_{ON} *[= 1/ (dI_D/dV_{DS})]* is extracted within the ohmic region of the measured IV characteristics.

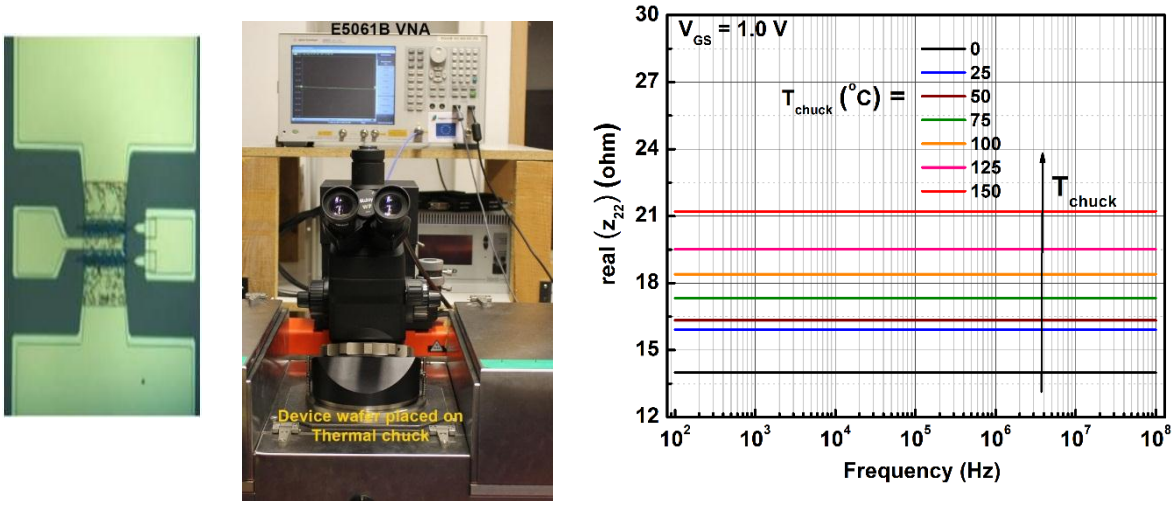
4.2.3. LF-S Parameter Measurements

The low frequency S-parameters measurements in the frequency range of 100 Hz to 100 MHz have been carried out using an Agilent E5061B network analyzer. The photograph of the device under test (DUT) and the LF measurement setup is shown in Fig. 4.11 (a).



(a) (b)

Fig. 4.10. Measured DC-IV output characteristics (I_D-V_{DS}): (a) for different V_{GS} bias between 1.0 V and -1.0 V at T_{chuck} = 25ºC. (b) for different T_{chuck} between 0ºC and 150ºC at V_{GS} = 1.0 V. Device dimensions: W_G = 2×100 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.



(a) (b)

Fig. 4.11. (a) Photograph of the DUT and the LF experimental setup. (b) Real part of Z_{22} parameter in reverse cold-FET condition for different T_{chuck} ranging between 0ºC and 150ºC and at V_{GS} = 1.0 V. Device dimensions: W_G = 2×100 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.

A detailed description about LF-S parameter measurements can be seen in chapter 3 (section 3.3.3). The S-parameters measurements have been performed at cold-FET condition [4.33] (V_{GS} > $V_{pinch\text{-}off}$ and V_{DS} = 0 V). The S-parameters measured are converted into the equivalent Z-parameters and after the addition of parasitic resistances and inductances, the Z_{22} parameters can be expressed as [4.33], [4.34]:

$$Z_{22} = R_s + R_d + R_{ch} + j\left(\omega L_s + \omega L_d - \frac{1}{\omega C_d} - \frac{1}{\omega C_s}\right) \quad (4.1)$$

Where R_s, R_d, and R_{ch} represent the source, drain and channel resistances, L_s and L_d are the parasitic source and drain inductances, and C_s and C_d represent the parasitic source and drain capacitances. Therefore, the on-resistance (R_{ON}) can be determined from the real part of the measured Z_{22} parameter and it is given by:

$$\mathrm{Re}\left(Z_{22}\right) = R_{ON} = R_s + R_d + R_{ch} \quad (4.2)$$

Fig. 4.11 (b) shows the measured real part of Z_{22} parameter of the 2×100 µm device for different T_{chuck} ranging between 0°C and 150°C at V_{GS} =1.0 V, respectively. The corresponding R_{ON} is determined as a function of V_{GS} and T_{chuck}, using the real part of the Z_{22} parameter.

4.2.4. Numerical TCAD Simulations

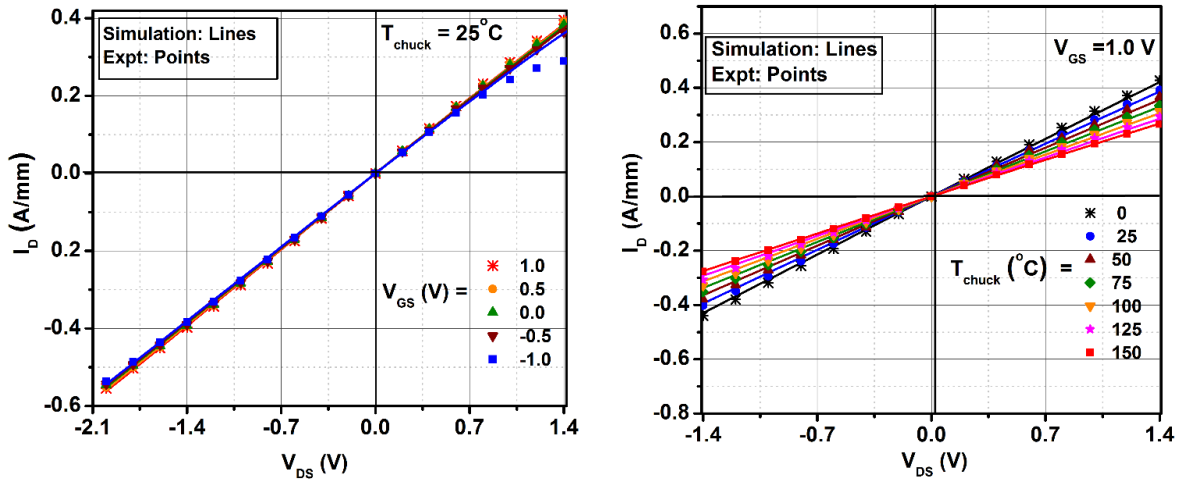
Two-dimensional physics based numerical simulations have been carried out using the commercially available TCAD Sentaurus software from Synopsys Inc. The calibration model described in section 4.1.3 is used for simulations. Temperature-dependent carrier mobility model and field-dependent Caughey-Thomas model [4.35] described in Chapter 3 (section 3.6.1) has been used for calibration of dc-IV characteristics as a function of temperature. Temperature dependence fitting parameters, α, β and γ values are assumed to be 1.7, 2.1 and 2.6, respectively for the GaN material. Moreover, based on our in-house measurements, the temperature-dependent ohmic source and drain contact resistances $R_C(T)$ are modeled using the following equation which is used in the simulation:

$$R_C(T) = R_C\left(T_{ref}\right) + \lambda\left(T - T_{ref}\right) \quad (4.3)$$

where $R_C(T_{ref})$ is the contact resistance (1.080 Ω-mm) at the reference temperature of 0°C and λ is the temperature dependence fitting parameter, whose value is 0.0026.

The simulation model is calibrated for the 2×100 µm device with L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm. Fig. 4.12 (a) shows the simulated and experimental DC output characteristics for V_{GS} values varying from +1.0 V to -1.0 V in 0.5 V steps and at T_{chuck} = 25°C. Similarly, Fig. 4.12 (b) shows the comparison of the simulated and experimental characteristics at V_{GS} =1.0 V and for varying T_{chuck} between 0°C and 150°C. The good agreement between the simulation results and the experimental data confirms the validity of the physical model calibration.

Therefore, R_{ON} is extracted using the simulation results and then compared with the experimental data in the next section.



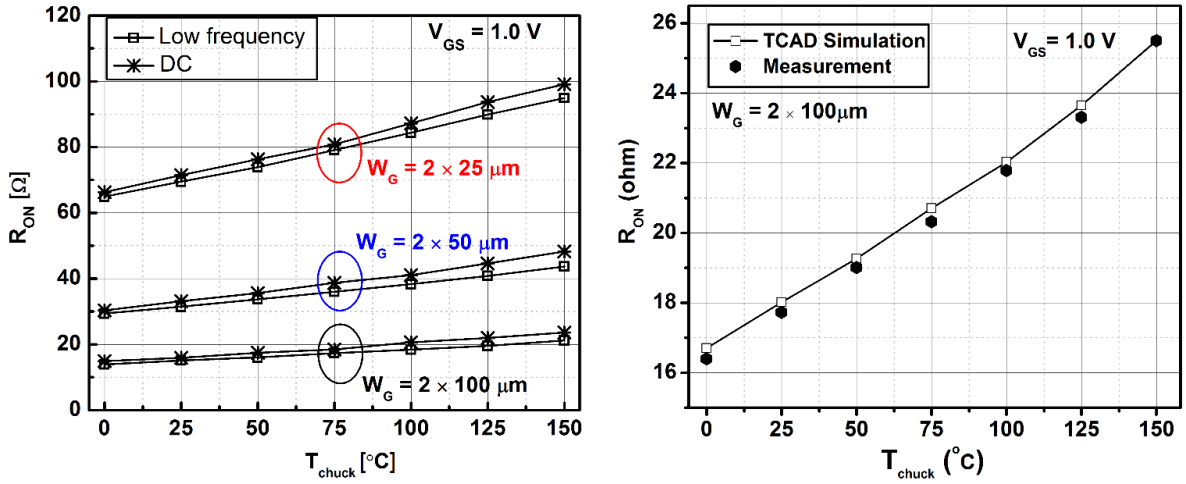
(a) (b)

Fig. 4.12. Comparison of the simulated (solid lines) and measured (symbols) DC-IV output characteristics: (a) for different V_{GS} biases between 1.0 V and -1.0 V at T_{chuck} = 25°C. (b) for different T_{chuck} between 0°C and 150°C at V_{GS} = 1.0 V. Device dimensions: W_G = 2×100 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.

4.2.5. Temperature Dependent R_{ON} Extraction

The R_{ON} extracted as function of temperature from the dc-IV and low frequency S-parameters measurements for the device dimensions of W_G = 2×100 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm at V_{GS} = 1.0 V is shown in Fig. 4.13 (a). Both measurements are performed at very low V_{DS}, implying that the measured characteristics are not affected by the traps activated due to the applied drain voltage, which has significant impact on R_{ON}. Therefore, the good agreement obtained between the two methods as shown in Fig. 4.13 (a) demonstrates that the values obtained are free from the influence of traps and constitute the reference data for comparison with TCAD simulations. However, under large signal working conditions it will be necessary to take into account the increase of R_{ON} values due to traps. In order to verify the R_{ON} extraction procedure, the measurements are repeated for various device widths of 2×25 and 2 × 50 µm, keeping all other device dimensions identical. The results obtained demonstrate that the extraction procedure remains valid for various device geometries (Fig. 4.13 (a)). It is a well-known fact that R_{ON} and the device width are inversely related. It can be seen from Fig. 4.13 (a), when the device width is increased by a factor of 2, the corresponding on-resistance of the device is scaled almost by the same factor. Fig. 4.13 (b) shows the comparison of R_{ON} extracted

from the DC simulation results and the measurement data for the 2×100 µm device. A good agreement is observed between the measurement and TCAD simulation for V_{GS} of +1.0 V in the temperature range of 0°C to 150°C.



(a) (b)

Fig. 4.13. R_{ON} as a function of T_{chuck}: extracted from DC and low frequency measurements for different geometries of AlN/GaN/AlGaN HEMTs on SiC and (b) Comparison of R_{ON} values extracted using TCAD simulations (solid line with open symbols) and measurement results (symbols) at V_{GS} = 1.0 V and T_{chuck} between 0 °C and 150°C. Device dimensions: W_G = 2×100 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.

4.2.6. Channel Sheet Resistance Extraction Methodology

The temperature dependent $R_{ON}(T)$ can be described as the sum of the parasitic series contact resistance $R_{se}(T)$ and the channel resistance $R_{ch}(T)$ as shown in Fig. 4.14 [4.36] . Here, $R_{se}(T)$ is the sum of the source (R_s) and drain (R_d) contact resistances. As shown in Fig. 4.14, the channel between source and drain can be subdivided into three regions: source-gate, underneath gate, and gate-drain region. Therefore, the total channel resistance can be expressed as a series combination of $R_{sh}L_{SG}/W_G$, $R_{sh}L_G/W_G$ and $R_{sh}L_{GD}/W_G$, where R_{sh} is the sheet resistance or square resistance (Ω/□) of the channel.

The resistance term ($R_{sh}L_G/W_G$) under the gate is a function of V_{GS}, due to the depletion of Schottky gate contact. For a constant gate bias, $R_{ON}(T)$ can be expressed as follows [4.37]:

$$R_{ON}(T) = R_{se}(T) + \left(\frac{L_{SG} + L_G + L_{GD}}{nW_G}\right) R_{sh}(T) \tag{4.4}$$

$$R_{sh}(T) = R_{sh}(T_{ref}) + \frac{dR_{sh}(T)}{dT}(T - T_{ref}) \tag{4.5}$$

$$R_{se}(T) = R_{se}(T_{ref}) + \frac{dR_{se}(T)}{dT}(T - T_{ref}) \tag{4.6}$$

where, L_{SG}, L_G, and L_{GD} are the source-gate, gate and gate-drain length, respectively. Following the linear variation of R_{ON} with temperature (Fig. 4.13), the $R_{sh}(T)$ and $R_{se}(T)$ can be expressed using a linear approximation as given in (4.5) and (4.6). Here, $R_{sh}(T_{ref})$ and $R_{se}(T_{ref})$ are the reference sheet resistance and contact resistance at a reference temperature T_{ref}, respectively. The source-drain length is given by, $L_{SD} = (L_{SG} + L_G + L_{GD})$. Differentiating (4.4) with respect to T,

$$\frac{dR_{ON}(T)}{dT} = \frac{dR_{se}(T)}{dT} + \left(\frac{L_{SD}}{nW_G}\right)\frac{dR_{sh}(T)}{dT} \tag{4.7}$$

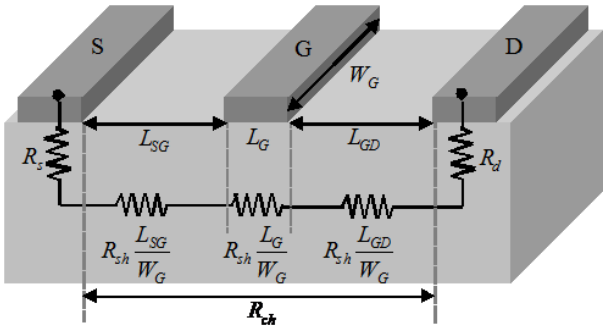


Fig. 4.14. Structure of the transistor showing the series contact resistance R_{se} (= R_s + R_d) and channel resistance R_{ch} [4.38].

The procedure for extracting sheet resistance and the series contact resistance using (4.4) – (4.7) is illustrated in Fig. 4.15 [4.37]. Referring to (4.5) and (4.6), it is clear that R_{sh} (T_{ref}) and R_{se} (T_{ref}) can be extracted at the reference temperature and for one particular V_{GS} using (4.4). The plot of R_{ON} (T_{ref}) against different L_{SD}/nW_G (Fig. 4.15) yields a straight line, whose slope and intercept gives the value of R_{sh} (T_{ref}) and R_{se} (T_{ref}). Similarly plotting R_{ON} as a function of temperature (Fig. 4.15) yields a straight line, whose slope gives dR_{ON}/dT. The dR_{ON}/dT extraction is repeated for different L_{SD}/nW_G and by plotting dR_{ON}/dT versus L_{SD}/nW_G yields a straight line (Fig. 4.15), whose slope is dR_{sh}/dT and the intercept is dR_{se}/dT. Hence, all the unknown parameters in (4.5) and (4.6) are now determined and by using these equations, R_{sh} (T) and R_{se} (T) can be calculated at any temperature within the measurement range of 0°C and 150°C. The aforementioned procedure can be repeated for different V_{GS} and therefore the sheet resistance and the parasitic contact series resistance can be extracted as function of temperature and gate-source bias voltage.

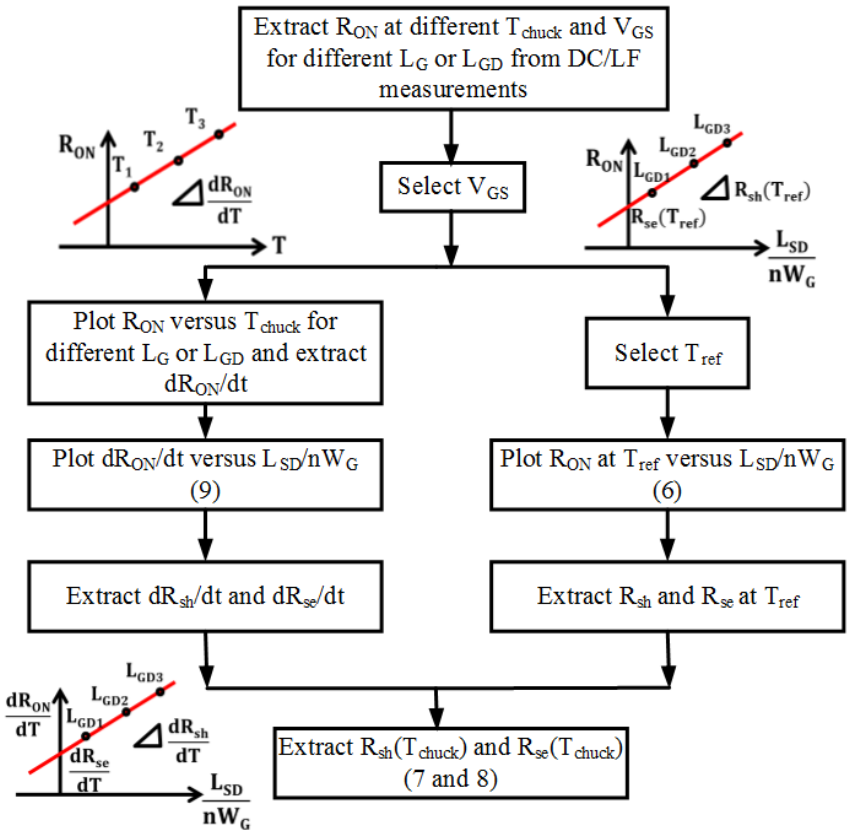
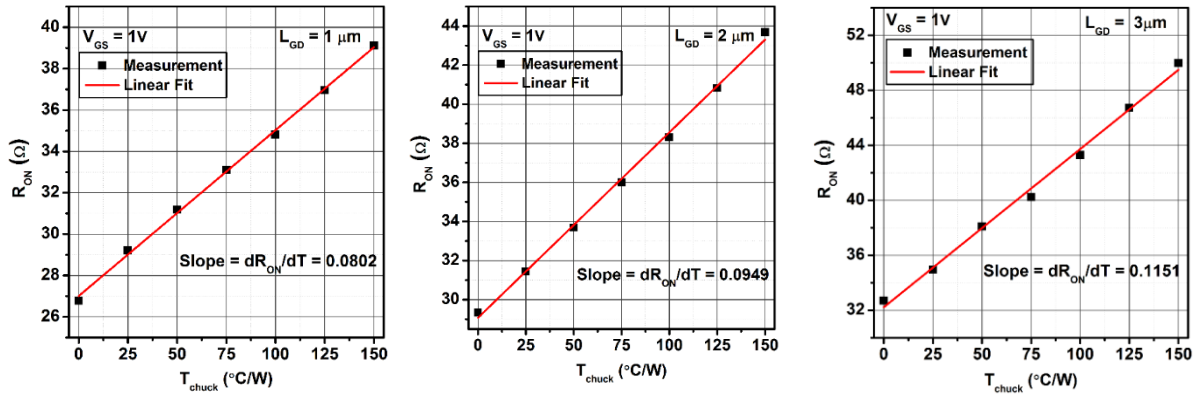


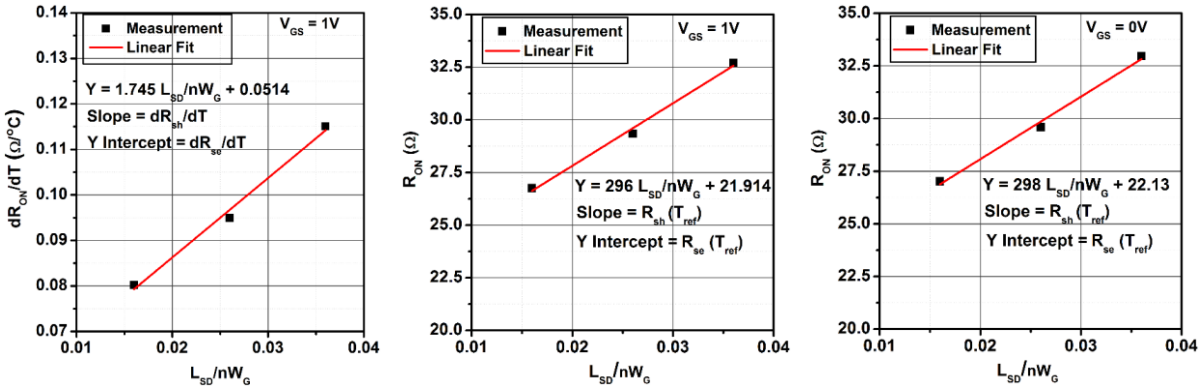
Fig. 4.15. Flowchart for extracting channel sheet resistance (R_{sh}) and series contact resistance (R_{se}).

4.2.7. Results and Discussions

Following the above described methodology, the extraction of $R_{sh}(T)$ and $R_{se}(T)$ is performed using $R_{ON}(T)$ data obtained from low frequency measurements of the devices with W_G of 2×50 µm, L_G of 0.2 µm, L_{SG} of 0.4 µm, and for different L_{GD} of 1.0, 2.0 and 3.0 µm, respectively. The extracted R_{sh}, R_{se}, dR_{sh}/dT and dR_{se}/dT at a T_{ref} of 0°C are shown in Fig. 4.16.



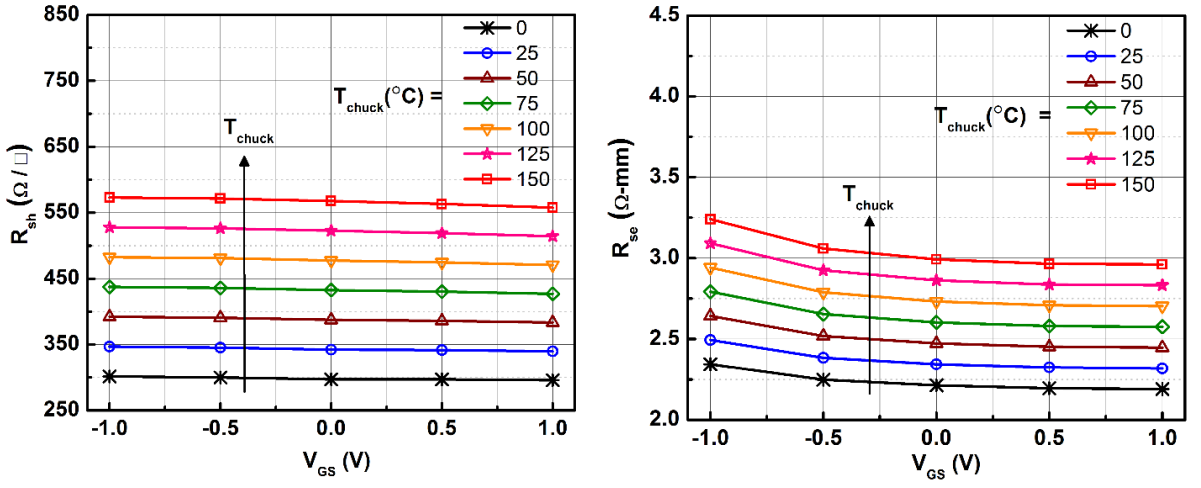
(a) (b) (c)



(d) (e) (f)

Fig. 4.16. LF S-parameters measurement at T_{ref} = 0°C and V_{GS} = 1 V: extraction of dR_{ON}/dT [(a), (b) and (c)] for different gate-drain distance, L_{GD} = 1, 2 and 3.0 µm, respectively, extraction of dR_{sh}/dT (d) and Extraction of R_{sh} and R_{se} : at V_{GS} = 1 V (e) and 0 V (f). Device dimensions: W_G = 2×50 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.

The corresponding extracted values are given as function of V_{GS} in Table 4.2. Fig. 4.17 (a) and 4.17 (b) show the extracted R_{sh} (Ω/□) and R_{se} (Ω-mm) as function of V_{GS} for different T_{chuck} values between 0°C and 150°C. It is worthwhile to note that the extracted values of R_{sh} at 25°C and for different V_{GS} are in reasonable agreement with the already reported value of 355 Ω/□ [4.10] for this device technology. A significant variation of resistance with temperature is found. On the other hand the devices under characterization exhibit a higher contact resistance.



(a) (b)

Fig. 4.17. Extracted (a) channel sheet resistance R_{sh} and (b) series contact resistance R_{se} as function of V_{GS} and T_{chuck} using LF measurements. Device dimensions: W_G = 2×50 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.

Table 4.2. Resistances and derivatives at different V_{GS} using LF S-parameter measurements.

V_{GS} (V)	Resistances at T_{ref} = 0°C and dR/dT			
	R_{sh} (Ω/□)	dR_{sh}/dT	R_{se} (Ω-mm)	dR_{se}/dT
-1.0	302	1.81	2.34	0.0060
-0.5	300	1.82	2.25	0.0054
0.0	298	1.80	2.21	0.0052
0.5	297	1.77	2.20	0.0051
1.0	296	1.75	2.19	0.0051

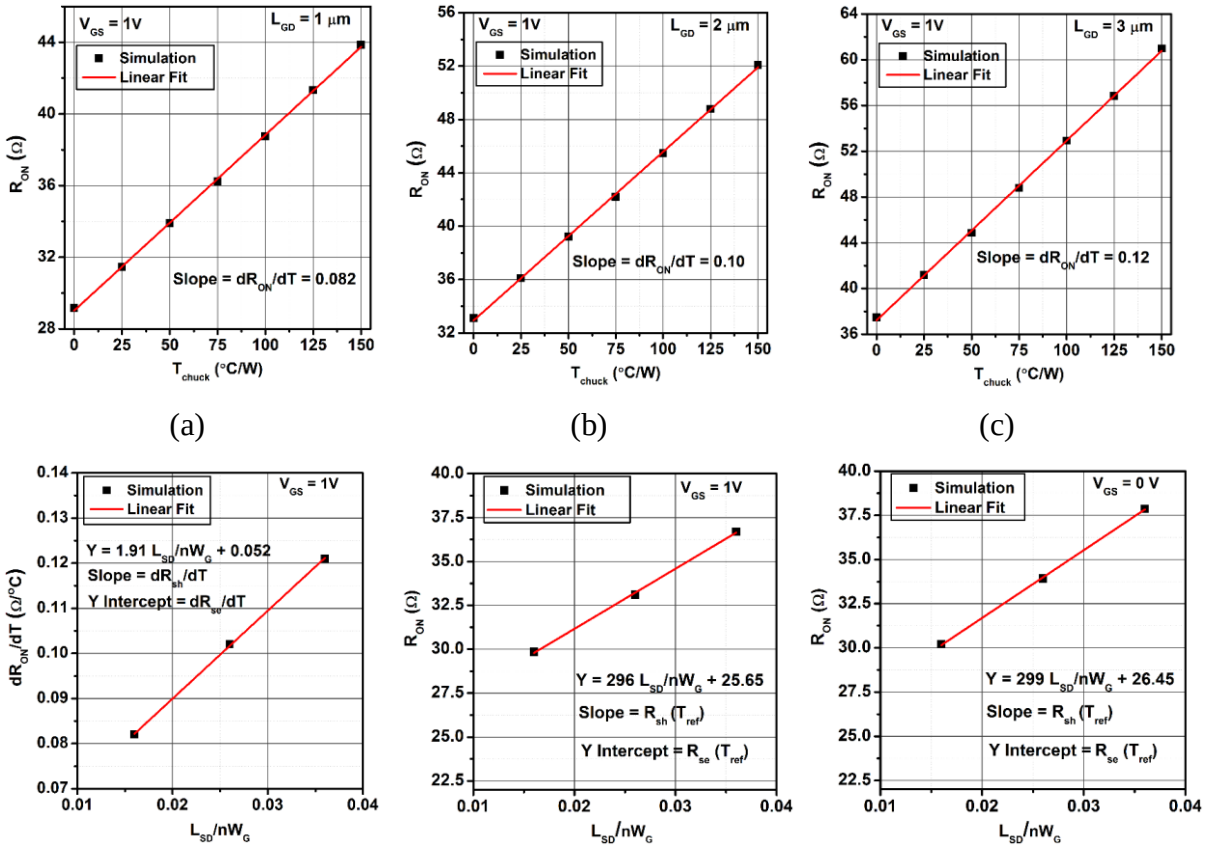
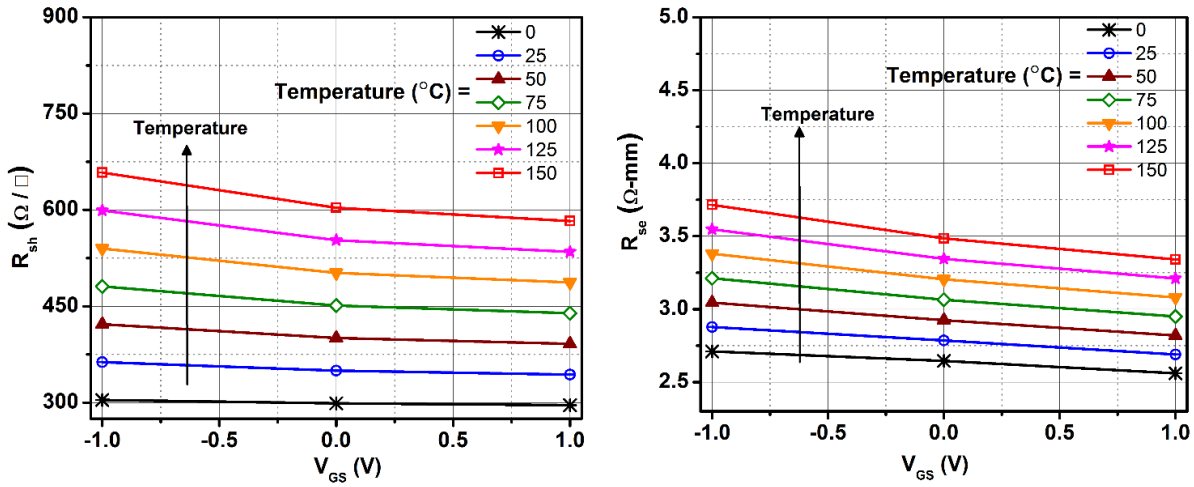


Fig. 4.18. TCAD dc-IV simulation at T_{ref} = 0°C and V_{GS} = 1 V: extraction of dR_{ON}/dT [(a), (b) and (c)] for different gate-drain distance, L_{GD} = 1, 2 and 3.0 µm, respectively, extraction of dR_{sh}/dT (d) and Extraction of R_{sh} and R_{se} : at V_{GS} = 1 V (e) and 0 V (f). Device dimensions: W_G = 2×50 µm, L_G =0.2 µm, L_{SG} =0.4 µm, and L_{GD} = 2 µm.

In order to verify the R_{sh} and R_{se} extraction methodology in physical simulations, devices with width of 2×50 µm, L_G of 0.2 µm, L_{SG} of 0.4 µm, and different L_{GD} of 1.0, 2.0 and 3.0 µm, respectively are used. The calibrated simulation model parameters of the 2×100 µm device are

used here for the simulations. From the simulated DC-IV characteristics, the R_{ON} values are extracted at different gate biases and temperatures. Then, using the proposed method (Fig. 4.15), the channel sheet resistance and series contact resistance as function of bias and temperature are determined. The extracted R_{sh}, R_{se}, dR_{sh}/dT and dR_{se}/dT at a T_{ref} of 0°C, using dc-IV TCAD simulations are shown in Fig. 4.18. Fig. 4.19 (a) and 4.19 (b) show the extracted R_{sh} (Ω/□) and R_{se} (Ω-mm) using the TCAD simulation results. The corresponding extracted resistances at T_{ref} of 0°C and for different gate biases are given in Table. 4.3. The variations in the extracted R_{sh} (Ω/□) and R_{se} (Ω-mm) between measurements and TCAD simulations (Fig. 4.17 and 4.19) are only due to the calibration error. In order to achieve a better match, the simulation model needs to be properly calibrated for the 2×50 µm devices, for different L_{GD} of 1.0, 2.0 and 3.0 µm, respectively.



(a) (b)

Fig. 4.19. Extracted (a) channel sheet resistance R_{sh} and (b) series contact resistance R_{se} as function of V_{GS} and T_{chuck} using TCAD simulations.

Table 4.3. Resistances and derivatives at different V_{GS} using TCAD simulations.

V_{GS} (V)	Resistances at T_{ref} = 0°C and dR/dT			
	R_{sh} (Ω/□)	dR_{sh}/dT	R_{se} (Ω-mm)	dR_{se}/dT
-1.0	304	2.36	2.71	0.0067
0.0	299	2.02	2.65	0.0056
1.0	296	1.91	2.56	0.0052

4.3. Summary

In the first part of this chapter, we systematically studied the influence of GaN channel traps on the performance of AlN/GaN/AlGaN HEMTs through two-dimensional TCAD numerical simulations. The simulation model is calibrated using the experimentally measured dc-IV characteristics and the calibrated TCAD simulation model is used for our traps study. Our simulation results indicate a significant influence of acceptor-like traps on the simulated dc-IV characteristics, whereas the donor-like traps have no considerable influence on the device performance. Moreover, it is demonstrated that deeper the energy level of acceptor-like traps, large the degradation in dc-performance of the device.

In the second part of this chapter, we first studied the temperature dependency of on-resistance R_{ON} of AlN/GaN/AlGaN HEMTs grown on SiC substrate, for various device geometries through DC and low frequency measurements. We have also presented the 2D numerical simulation results for the on-resistance extraction of 2×100 µm device. A good agreement is achieved between the simulated and extracted R_{ON} for the temperature range of 0°C to 150°C. Then, we have proposed a simplified methodology to extract the temperature dependence of series contact resistance and channel sheet resistance of GaN based HEMTs. The proposed methodology has been successfully applied on 2×50 µm AlN/GaN/AlGaN HEMT devices, for various gate-source bias voltages and the corresponding $R_{sh}(T)$ and $R_{se}(T)$ are extracted. Two-dimensional TCAD device simulations have been also carried out for the same device dimensions and the temperature dependency of channel and contact resistances are extracted.

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Chapter 5

Thermal Characterization, Simulation and Modeling of AlN/GaN/AlGaN HEMTs

Based on Publication:

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Chapter 5. Thermal Characterization, Simulation and Modeling of AlN/GaN/AlGaN HEMTs

5.1. Introduction

In recent years, AlN/GaN HEMT technology has attracted a great deal of attention for high power microwave and mm-wave applications [5.1] because of its superior performance [5.1] compared to conventional AlGaN/GaN HEMT devices. Indeed, this device technology has already delivered many of the promises made over the last few years [5.2], [5.3] , however the self-heating and charge-trapping effects still remain as a critical factor in limiting the device performance and its reliability. Moreover, the reliability of the device depends on the operating channel temperature [5.4]. The channel temperature can reach several hundred degrees above ambient base temperature when the device is operating in high power condition. It degrades the maximum power density achievable and accelerates the device failure [5.4]. The thermal resistance (R_{TH}) plays a significant role in estimating the channel temperature of the device. Lower thermal resistance can enhance the device performance and indeed proved to be useful in accomplishing the effective thermal management. Furthermore, the thermal resistance of the device depends on the thermal conductivity of the substrate material. The commercially available GaN HEMT devices are grown either on Silicon carbide (SiC) or Si substrates. The GaN HEMTs grown on SiC substrate offer a lower thermal resistance, owing to the high thermal conductivity of SiC. However, the SiC substrate is extremely expensive and the availability of the large size wafers is limited. Hence, Si substrate is considered as a suitable alternative due to its low cost and easy availability [5.5]. The higher thermal resistance associated with the lower thermal conductivity of Si substrate would significantly affect the device performance, especially at high power dissipation condition. Therefore, the systematic analysis of thermal behavior of the GaN HEMT devices grown on Si and SiC substrates is an active research area to explore.

A number of experimental techniques such as Raman spectroscopy, electrical measurement techniques, IR thermal imaging, thermo-reflectance thermography and infrared microscopy have been used with some extent but are limited either by spatial or temperature resolution [5.4]. Numerical simulation offers also an efficient alternate approach to evaluate the thermal behavior of devices [5.6] [5.7]. However, electro-thermal simulations based on the finite element method (FEM) are time consuming and rather complex. Therefore, in this chapter, we focus mainly on the thermal behavior of AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrates through pulsed I-V measurements and three-dimensional TCAD based thermal

simulations. In addition, AlN/GaN/AlGaN HEMT devices grown on sapphire substrate have also been studied using 3D-TCAD thermal simulations.

5.2. Thermal Parameters Definition

The temperature rise in integrated circuits (ICs) occurs due to the following reasons [5.8]: (i) Self-heating effects (SHE) in the device due to dc-power dissipated inside the device and (ii) thermal coupling between neighboring components. The SHE is the most dominant one and this causes the variation of temperature inside the device. However, the distribution of temperature inside the device is non-uniform. Moreover, this SHE causes the transfer of heat from the heat source (channel region) to the back side of the substrate. In general, the back side of the substrate is connected to the external environment and the temperature is ideally assumed to be ambient temperature. Therefore, the transfer of heat to this substrate region results in temperature rise inside the device above the ambient temperature. The amount of heat transfer to the substrate is strongly dependent on the thermal conductivity of the substrate material used. Moreover, the heat flow from the heat source to the top of the device via interconnect metallization is assumed to be negligible [5.8].

5.2.1. Thermal Resistance (R_{TH})

The temperature rise influences the device/circuit behavior is strongly dependent on the power dissipated inside the device. It is more convenient to represent a quantity that can describe the steady-state thermal behavior, independent of the dissipated power. Therefore, the thermal resistance (R_{TH}) can be defined as the ratio of temperature increase (ΔT) over ambient temperature (T_{amb}) to dissipated power (P_{diss}) [5.9]:

$$R_{TH} = \frac{T_j - T_{amb}}{P_{diss}} = \frac{\Delta T}{P_{diss}} \tag{5.1}$$

Where T_j is the junction temperature, T_{amb} is the ambient temperature and P_{diss} is the power dissipated in the device. R_{TH} is the thermal resistance (also called self-heating thermal resistance) of the device that depends on the material properties and geometry of the fabricated device structure.

The power dissipation in the device can be calculated using the following formula:

$$P_{diss} = I_D.V_{DS} \tag{5.2}$$

Where I_D and V_{DS} are the drain current and drain-source voltage, respectively.

The thermal resistance is sufficient to describe the relationship between temperature and the power dissipated in the device under steady state conditions. However, for transient response, the thermal capacitance (C_{TH}) is used and it can be expressed using [5.10]:

$$C_{TH} = \rho.c.V \tag{5.3}$$

Where c is the specific heat capacity, ρ is the density and V is the volume of the material.

5.2.2. Thermal Impedance (Z_{TH})

It is a physical quantity that can be used to model the dynamic behavior of the device temperature. In time domain, it can be defined as the thermal transient response to the unitary power step. For instance, if the dissipated power increases instantaneously from 0 to P_{diss} at time, t = 0, the thermal impedance can be given by [5.11]:

$$Z_{TH} = \frac{T_j(t) - T_{amb}}{P_{diss}} = \frac{\Delta T(t)}{P_{diss}} \tag{5.4}$$

Where $T_j(t)$ is the time evolution of junction temperature during the applied power step.

The thermal resistance corresponds to the steady state value of $Z_{TH}(t)$:

$$Z_{TH}(+\infty) = R_{TH} \tag{5.5}$$

The two another major factors which can describe the dynamic thermal behavior, are the rise time, t_R and the thermal cut-off frequency f_{TH}. The rise time represents the time interval between two points where the transient response attains the 10% and 90% of the steady state R_{TH} value, respectively. The thermal cut-off frequency is defined as the frequency at which the magnitude of Z_{TH} reduces to the value of $R_{TH}/ (2)^{1/2}$.

5.2.3. Thermal Conductivity (κ)

In general, thermal conductivity is assumed as a constant parameter for a material. However, this assumption is not completely true for many semiconductor materials since they show a temperature dependence of thermal conductivity. Therefore, the temperature dependent thermal conductivity can be expressed by using the following equation:

$$\kappa(T) = \kappa_0 . \left(\frac{T}{T_0}\right)^{-\alpha} \tag{5.6}$$

Where κ_0 is the thermal conductivity at the reference temperature T_0 = 300 K, T is the temperature and α is the temperature-dependent fitting parameter.

In TCAD Sentaurus simulator, the temperature dependent thermal conductivity is given by the following equation [5.12]:

$$\kappa(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2} \tag{5.7}$$

For silicon, κ_a = 0.03 cmKW^{-1}, κ_b = 1.56 ×10^{-3} cmW^{-1} and κ_c = 1.65 ×10^{-6} cmW^{-1}K^{-1}. The range of validity is from 200 K to well above 600 K. The temperature independent thermal conductivity of silicon can be defined with the following parameters: κ_a = 1.54 cmKW^{-1}, κ_b = 0 cmW^{-1} and κ_c = 0 cmW^{-1}K^{-1}, respectively.

5.2.4. Lattice Heat Capacity (C_L)

In TCAD Sentaurus simulator, the temperature dependent lattice heat capacity is modeled by the following empirical function [5.12]:

$$C_L = cv + cv\_b.T + cv\_c.T^2 + cv\_d.T^3 \tag{5.8}$$

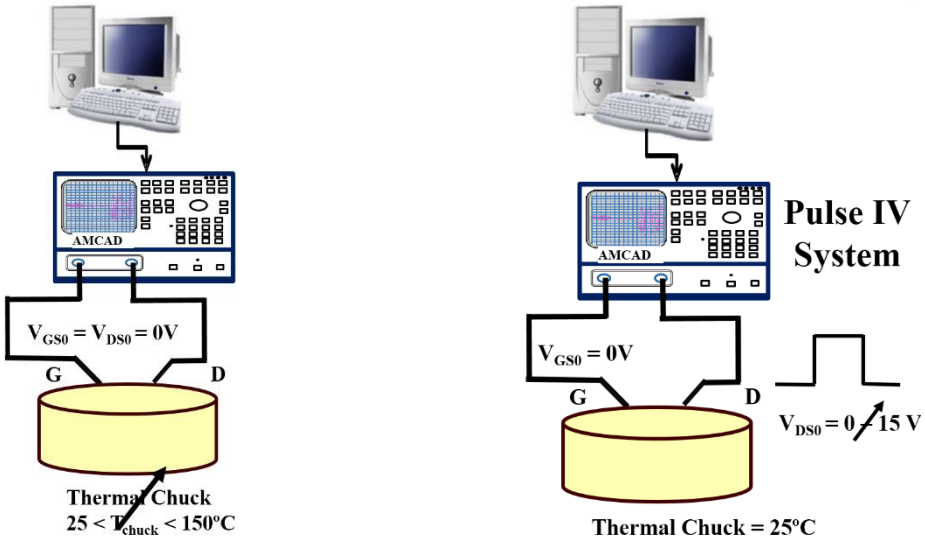
For silicon, a constant lattice heat capacity can be defined using the following parameters: cv = 1.63 J/Kcm^3, cv_b = 0 J/K^{2}cm^3, cv_c = 0 J/K^{3}cm^3 and cv_d = 0 J/K^{4}cm^3, respectively.

5.3. Experimental Structure

The AlN/GaN/AlGaN heterostructure field-effect transistors (HFETs) were grown by metal-organic chemical vapor deposition (MOCVD) on a 550-µm Si and SiC substrates. The epilayers consist of a 1.5-µm thick $Al_{0.08}Ga_{0.92}N$ buffer layer, 150-nm thick GaN channel layer followed by a 6-nm ultrathin AlN barrier layer and 3-nm in-situ grown Si_3N_4 cap layer. Ni/Au Schottky gate contact and Ti/Al/Mo/Au metal stack for ohmic source and drain contacts were deposited directly on top of the AlN barrier layer by etching the in-situ Si_3N_4 layer. The devices with different gate widths, W_G of 25 µm, 50 µm and 100 µm, each with two fingers (n=2) are fabricated on the same wafer. The gate length L_G of the devices is 0.2 µm, source-gate separation (L_{SG}) is fixed to 0.4 µm and gate-drain distances (L_{GD}) is 2 µm, respectively.

5.4. Thermal Resistance (R_{TH}) Extraction Using On-wafer Pulsed I-V Measurements

In this work, the method proposed in [5.13] is used to extract the thermal resistance (R_{TH}) of the devices using on-wafer pulsed I – V measurements. The measurement technique consists of two steps [5.9] [5.13]: a calibration step (Fig. 5.1 (a)) and a measurement step (Fig. 5.1 (b)). In the calibration step, the quiescent point selected is V_{GS} = V_{DS} = 0 V in order to ensure that there is no dissipated power in the device. Hence, at this condition the channel temperature and chuck temperature are considered to be almost identical.

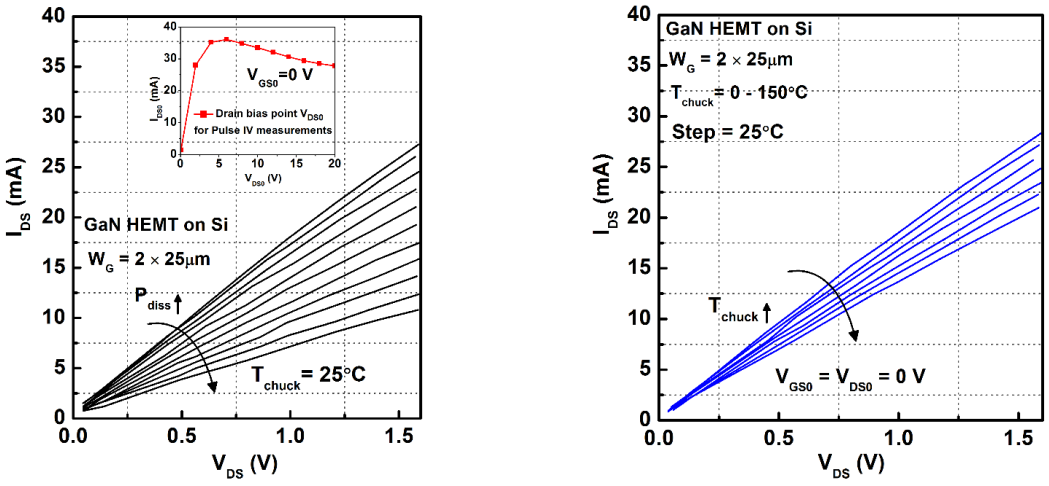


(a) (b)

Fig. 5.1. Pulsed I-V measurement setup: (a) calibration step and (b) measurement step.

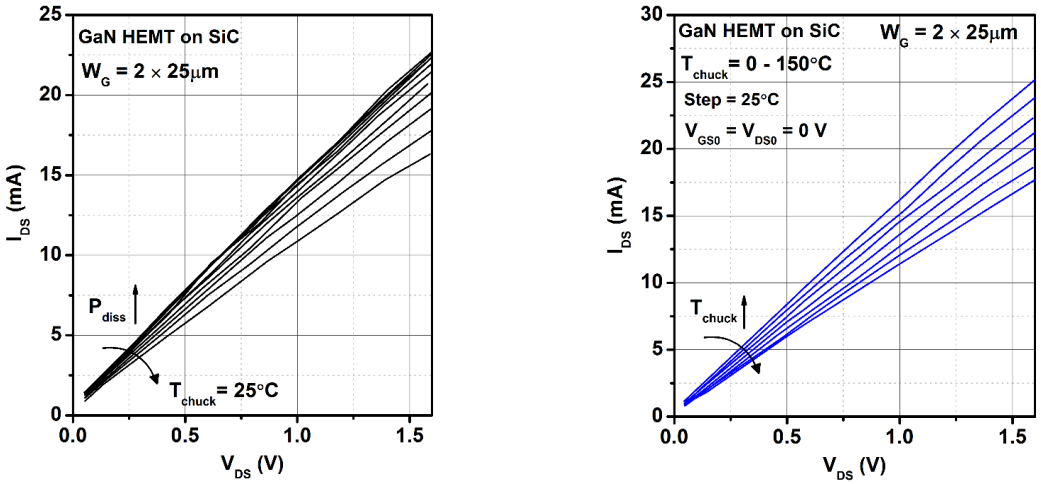
The pulsed I – V characteristics of the devices have been measured for different chuck temperature (T_{chuck}) ranging between 0ºC and 150ºC. The on-resistance (R_{ON}) is extracted from the slope of the linear region of the measured characteristics. In the measurement step, T_{chuck} and V_{GS} are held constant (T_{chuck} =25ºC, V_{GS} = 0V) and by varying the V_{DS}, the device dissipates a different amount of power by self-heating effects. At this condition, the R_{ON} is measured as a function of power dissipation (P_{diss}).

Fig. 5.2 and Fig. 5.3 show the pulsed I – V measurement characteristics of the 2×25 µm HEMT device grown on Si and SiC substrates as a function of P_{diss} and T_{chuck}. Similar measurements have been performed for 2×50 µm and 2×100 µm devices grown on Si substrate and the corresponding R_{ON} has been extracted.



(a) (b)

Fig. 5.2. Pulsed output characteristics (I_D-V_{DS}) at different bias points (P_{diss}) (a) and different T_{chuck} (b) for the HEMT grown on Si substrate. Device dimensions: W_G = 2×25 µm, L_G =0.2 µm, L_{SG} =0.4 µm and L_{GD} = 2 µm.



(a) (b)

Fig. 5.3. Pulsed output characteristics (I_D-V_{DS}) at different bias points (P_{diss}) (a) and different T_{chuck} (b) for the HEMT on SiC substrate. Device dimensions: W_G = 2×25 µm, L_G =0.2 µm, L_{SG} =0.4 µm and L_{GD} = 2 µm.

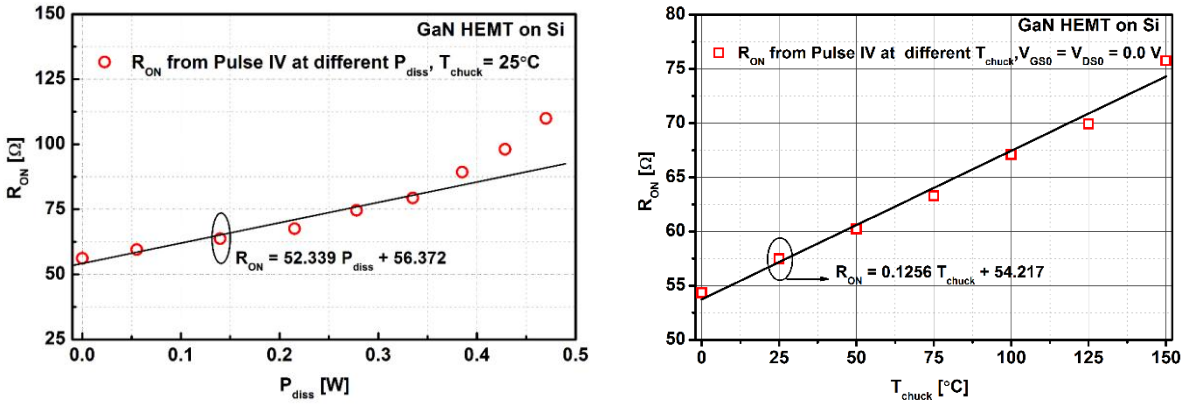
The variation of extracted R_{ON} as a function of T_{chuck} and P_{diss} for 2×25 µm HEMT devices are shown in Fig 5.4 and 5.5, respectively. For higher values of power dissipation (P_{diss}) in the device, R_{ON} follows a non-linear relationship with P_{diss} and this is due to the significant trapping effects occuring in the device [5.9]. Following the linear variation of R_{ON} with temperature and power dissipation, the R_{ON} can be expressed using the following equations as in [5.9]:

$$R_{ON}(\Delta T) = R_{ON}(T_0) + \frac{dR_{ON}}{dT}\Delta T \tag{5.9}$$

$$R_{ON}(P_{diss}) = R_{ON}(0) + \frac{dR_{ON}}{dP_{diss}}P_{diss} \tag{5.10}$$

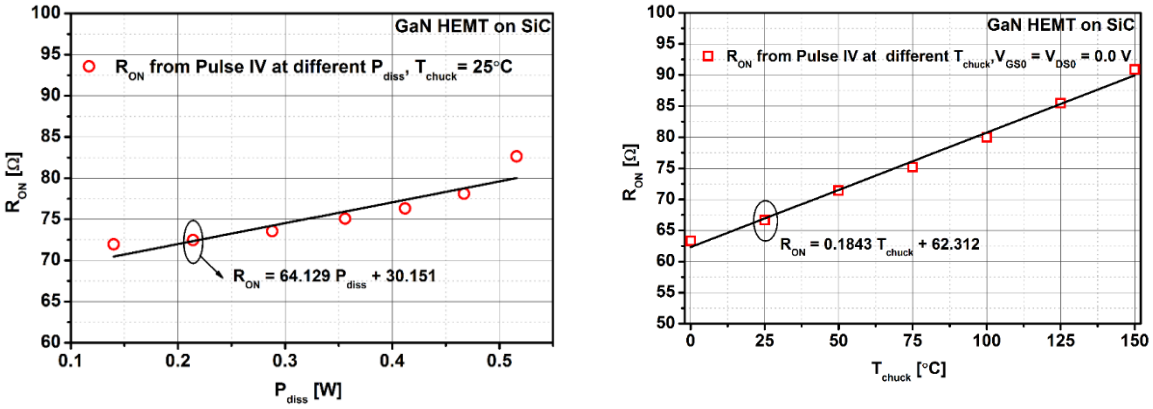
where reference temperature, T_0 = 25ºC represent the zero power dissipation condition and ΔT = T- T_0. Since T_0 corresponds to zero dissipated power, the thermal resistance can be extracted using equations (5.9) and (5.10) as follows [5.9]:

$$R_{TH} = \frac{\Delta T}{P_{diss}} = \left(\frac{dR_{ON}}{dP_{diss}}\right) / \left(\frac{dR_{ON}}{dT}\right) \tag{5.11}$$



(a) (b)

Fig. 5.4. Extracted R_{ON} at different P_{diss} (a) and different T_{chuck} (b) for HEMT grown on Si substrate. Device dimensions: W_G = 2×25 µm, L_G =0.2 µm, L_{SG} =0.4 µm and L_{GD} = 2 µm.



(a) (b)

Fig. 5.5. Extracted R_{ON} at different P_{diss} (a) and different T_{chuck} (b) for HEMTs on SiC substrate. Device dimensions: W_G = 2×25 µm, L_G =0.2 µm, L_{SG} =0.4 µm and L_{GD} = 2 µm.

The extracted thermal resistance (R_{TH}) for various HEMT devices grown on Si and SiC substrate is shown in Fig. 5.6.

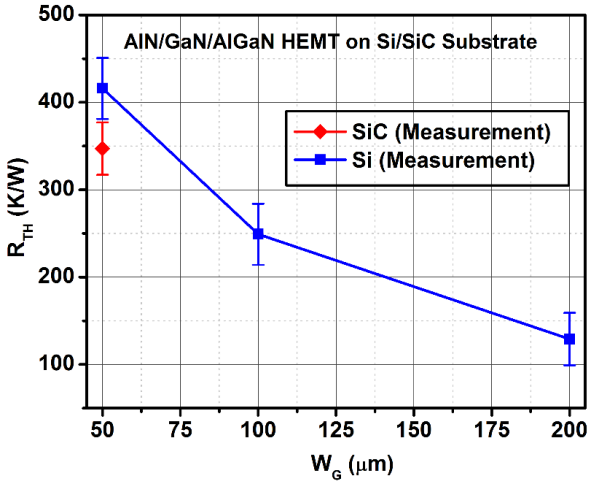


Fig. 5.6. Extracted R_{TH} as a function of device width for AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrate.

5.5. TCAD Thermal Simulation Methodology

The most accurate means of estimating the R_{TH}, heat flux and temperature is possible through the use of finite-element simulations [5.6]. The most commonly used simulation tool for performing thermal and electro-thermal simulations is the ANSYS software. However, TCAD Sentaurus tool is also equally capable of performing both thermal and electro-thermal simulations. Moreoever, in this thesis work, TCAD Sentaurus simulation tool [5.12] has been consistently used for all our simulations. Therefore, thermal simulations presented in this chapter also utilizes TCAD Sentaurus tool. It provides an efficient way of analyzing the heat diffusion mechanism, as heat is generated self-consistently within the device. In general, the TCAD simulation model can solve self-consistently the basic Poisson's equation along with the lattice heat flow equation. In this work, instead of solving the Poisson's equation to generate the heat dissipation inside the device, we have assumed an external heat source across the channel region to generate the required heat dissipation. The current density ($J_{n,p}$) involving temperature gradient, electron and hole quasi-Fermi potential can be expressed as [5.14]: $J_{n,p} = nq\mu_{n,p}(\nabla\Phi_{n,p} + P_{n,p}\nabla T)$. Here $\mu_{n,p}$ represent the electron and hole mobilities, $\Phi_{n,p}$ is the quasi-Fermi potential for electrons and holes respectively and $P_{n,p}$ represent the absolute thermoelectric power. The second term appears due to the non-uniform distribution of temperature inside the device. This gives rise to the current flow owing to the temperature gradient. The temperature distribution due to the self-heating can be calculated by solving the following lattice heat flow equation [5.14]:

$$C_L \frac{\partial T}{\partial t} - \nabla.\kappa\nabla T = -\nabla\left[\left(P_n T + \Phi_n\right)J_n + \left(P_p T + \Phi_p\right)J_p\right] \quad (5.12)$$

where κ and C_L represents the thermal conductivity and lattice heat capacity of the material. The function T denotes the temperature of the body. In our simulations, we have considered only the thermal phenomenon inside the device structure. Moreover, we assume that the device body obeys the heat equation and it generates its own heat (H) at the specific place called "heat source". Therefore, the temperature T satisfies the following equation [5.8], [5.15]:

$$C_L \frac{\partial T}{\partial t} - \nabla.\kappa\nabla T = H \quad (5.13)$$

where H can be the steady state, transient or dynamic power generated by the heat generator. The generated heat is applied at the heat source, which then dissipates the heat into the device structure obeying the heat flow mechanism.

The following boundary conditions are assumed in the simulations:

(i) The outer surface of the Si/SiC block is considered to be adiabatic and therefore, no heat flows from the device to the external surroundings.

(ii) The back-side of the wafer is an isothermal surface and initially kept at ambient temperature (300 K)

(iii) The heat transport from metallization to external surroundings is not considered for simplifying simulation.

5.6. Thermal Resistance (R_{TH}) Extraction Using TCAD Simulations

5.6.1. Device Structure

The physical structure of the AlN/GaN/AlGaN HEMTs grown on Si,SiC or sapphire substrate is shown in Fig. 5.7. The enlarged view detailing the different regions of the device is shown in Fig. 5.8 (a). The device structure is symmetric with respect to X-axis and therefore half of the device structure is used for simulations. The device has been placed on a semi-infinite Si, SiC or sapphire block and the thickness of the Si/SiC/sapphire-block is assumed to be same as the wafer thickness. The device is composed of several layers as shown in Fig. 5.8 (b). The device has two fingers, with source length (L_S) of 24 µm, gate-source separation (L_{SG}) of 0.4 µm, gate length (L_G) of 0.2 µm, gate-drain distance (L_{GD}) of 2.0 µm and drain length (L_D) of 13.36 µm respectively. The simulations are performed for three device widths, W_G of 25, 50 and 100 µm, respectively. The heat source is placed at the interface between AlN barrier and

GaN channel region, whose length (L_{HS}) is assumed to be twice the gate length of the device. The width of the heat source is assumed similar to the device width, respectively.

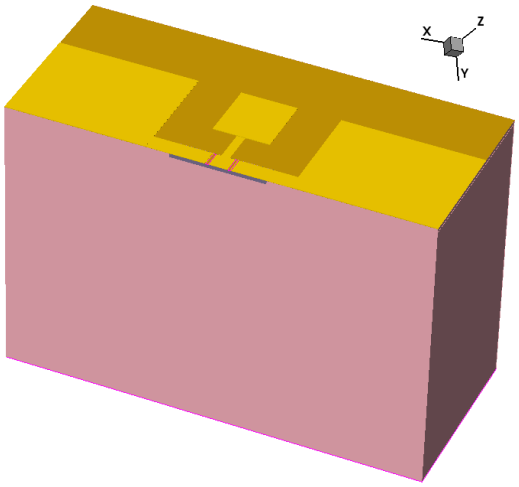
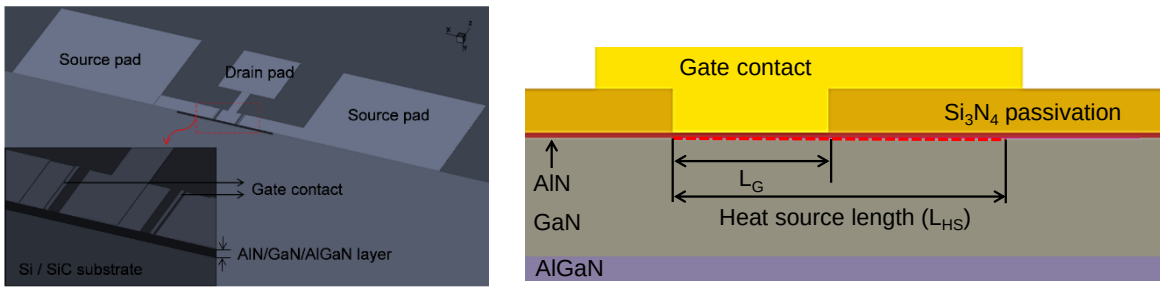


Fig. 5.7. Half of RF test structure of AlN/GaN/AlGaN HEMT grown on Si/SiC/Sapphire substrate.



(a) (b)

Fig. 5.8. (a) Detailed view of each regions of the AlN/GaN/AlGaN HEMT device structure (b) Enlarged view describing the epitaxial layers of device and also the placement of heat source at the AlN/GaN interface..

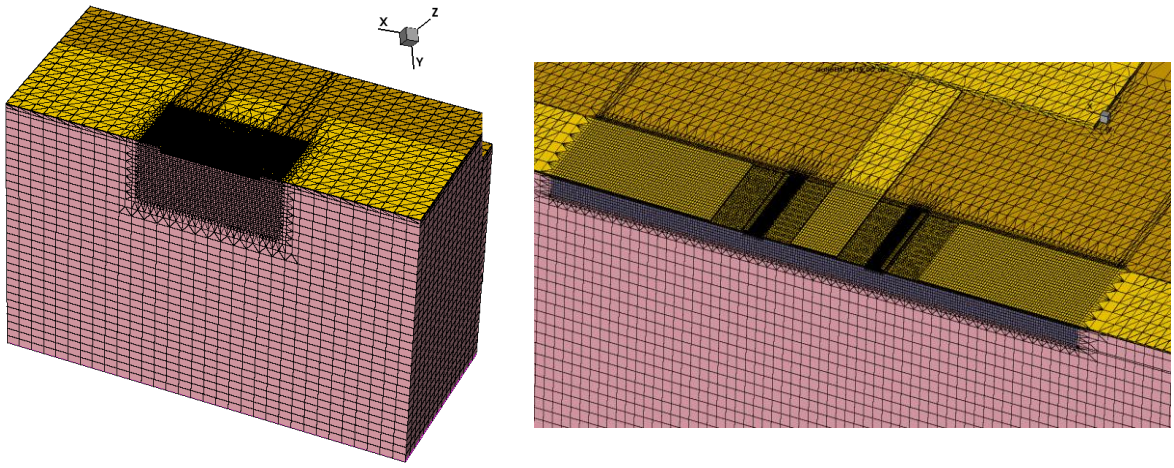
Meshing the device structure is an important aspect of device simulation. The mesh density should be fine at the device regions where the lattice temperature ($T_{Lattice}$) and heat flux (F_{Heat}) gradients are expected to be very high. Therfore, the meshing of the device has been optimized with the following conditions:

(i) Heterojunction interface between different materials

(ii) Heat source region and region close to the heat source.

(iii) Regions where the thermal gradients are expected to be high.

Moreover, the mesh density has been optmized in every region in order to decrease the simulation time with sufficient accuracy. Fig. 5.9 (a) and 5.9 (b) show the mesh refinement of the complete device and the region close to the placement of heat source. A higher mesh density is clearly observable around the heat source regions where the thermal gradients are generally high.



(a) (b)

Fig. 5.9. Mesh refinement in TCAD thermal simulation: (a) complete device structure (b) region around the heat source.

Table 5.1. Thermal conductivity and layer thickness of the materials used in thermal simulations.

Material	**Thermal Conductivity [W/cm-K]**	**Thickness [µm]**
AlN	2.85	0.006
GaN	1.3	0.15
AlGaN	0.4	2.5
Si_3N_4	0.027	0.056
Gold	3.15	0.256 (gate contact), 0.5 (GSG pad)
Si	1.54	550
SiC	4.55	550
Sapphire	0.35	550

We assume a temperature independent thermal conductivity (κ) and specific heat capacity (C_V) such that the physical simulations are linear. Table. 5.1 gives the thermal conductivity and layer thickness of the different materials used in the thermal simulations.

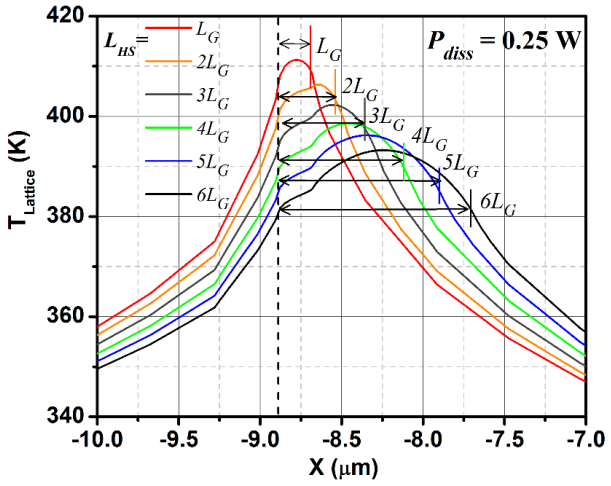
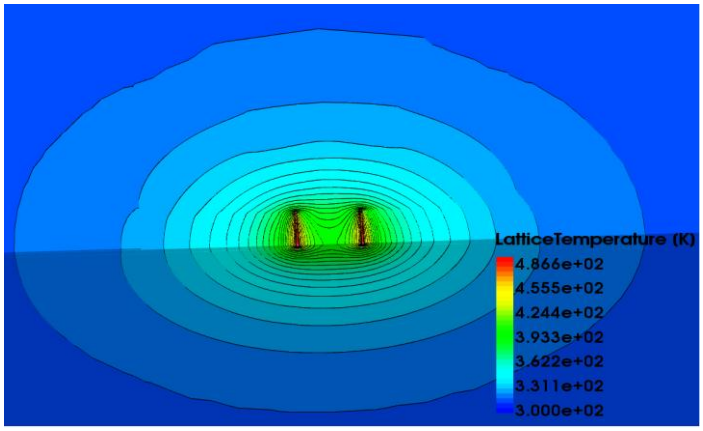


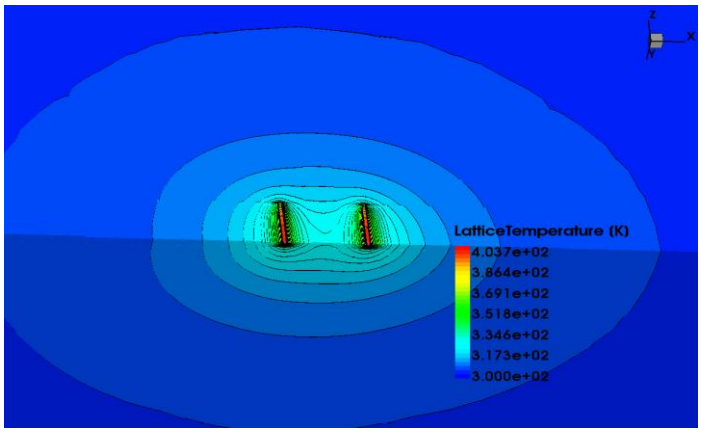
Fig. 5.10. Lattice ($T_{Lattice}$) and peak temperature variation for different L_{HS} in Si substrate.

In real operating conditions, when both the drain and gate biases are applied, the temperature of two-dimensional electron gas (2DEG) below the gate and drain-side gate edge increases due to the induced high local electric field. Several simulations have been carried out to optimize the length of the heat source (L_{HS}) whereas the width of the heat source (W_{HS}) is considered to be the same as the gate width (W_G). Fig. 5.10 shows the variation of lattice temperature ($T_{Lattice}$) along the transverse direction through the middle of the heat-source1 for the applied dc power of 0.25 W. The different lengths of heat source (L_{HS}= L_G, 2 L_G, 3 L_G, 4 L_G, 5 L_G and 6 L_G) have been considered from the source-side gate edge towards drain-side in order to achieve a match between the simulated and experimentally measured thermal resistance. A good compromise is obtained only when the L_{HS} is chosen to be twice the gate length of the device. This signifies the location of maximum electric field and therefore the hot spot is at the drain-side gate edge. Alternatively, if we allow the simulator to solve equation (5.12), it computes the heat dissipation area accordingly and therefore the optimization of L_{HS} is not necessary. However, the simulation time will be very high.

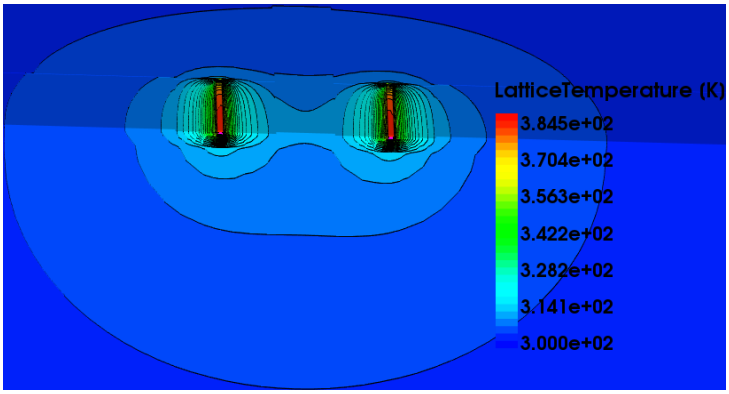
The steady state distribution of lattice temperature ($T_{Lattice}$) inside the HEMT grown on Si/SiC/Sapphire substrate is shown in Fig. 5.11. The applied dc power is 0.125 W per heat source and the device width is 50 µm.



(a)



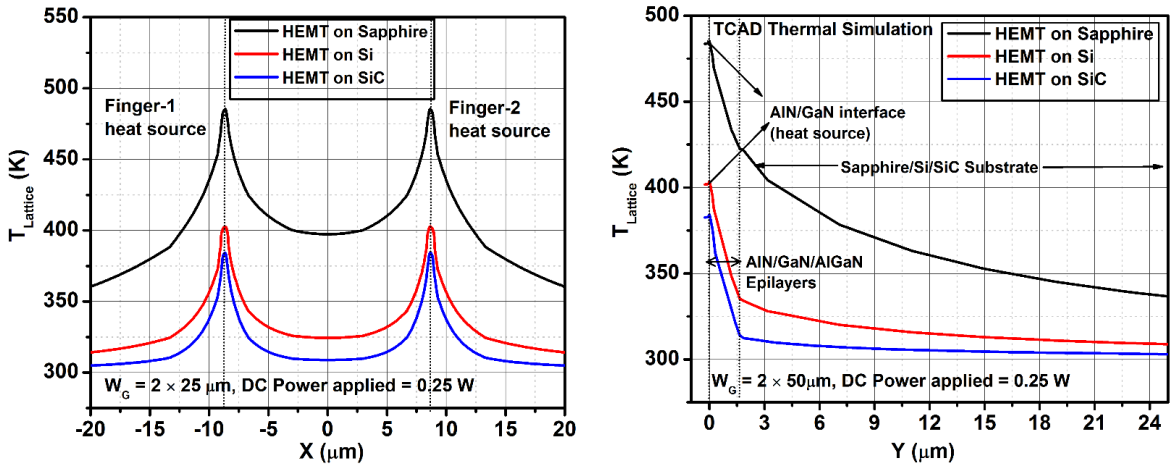
(b)



(c)

Fig. 5.11. Lattice temperature distribution at steady state condition for the applied DC power of 0.125 W per heat source of AlN/GaN/AlGaN HEMT on (a) Sapphire, (b) Si and (c) SiC substrate and with device width, W_G = 2×25 µm.

One-dimensional orthogonal cut is made (along X and Y axis as shown in Fig. 5.11) through the middle of the "heat source" in order to compare the variation of $T_{Lattice}$ between different substrates and this has been illustrated in Fig. 5.12 (a) and 5.12 (b), respectively. The substrate region clearly influences the thermal gradient. Note that, the higher thermal conductivity of the SiC substrate results a faster heat flow compared to sapphire and Si substrate.



(a) (b)

Fig. 5.12. Lattice temperature variation along the transverse direction, X (a) and Y (b) through the middle of heat source in AlN/GaN/AlGaN HEMT on different substrates, with W_G = 2×25 µm and for the applied dc power of 0.25 W).

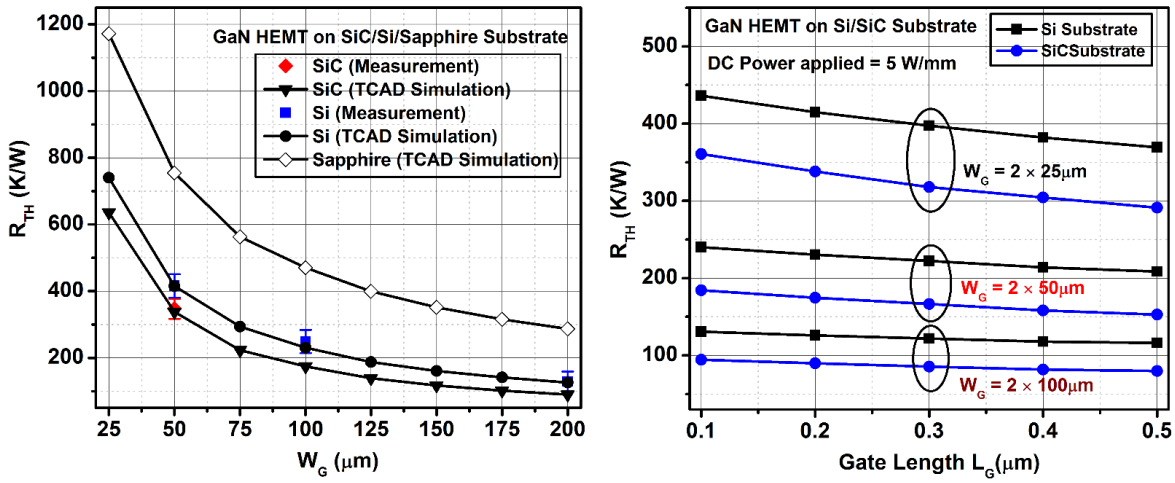
A significant difference in finger temperature is observed between different devices. It is worthwhile to note that for the same applied dc power, the lattice temperature at the epilayers/substrate interface is higher in case of Sapphire substrate when compard to Si and SiC substrate (Fig. 5.12 (b)). The ratio of increase in the lattice temperature at this interface is proportional to the ratio of the thermal conductivity values of materials. The respective ratio values are given in Table 5.2.

Table 5.2. Ratio of thermal conductivity of different substrate materials and the associated lattice temperature obtained in thermal simulations.

Thermal conductivity ratio:	**Simulated lattice temperature ratio:**
$\Delta K\|_{SiC/Si} = \frac{4.55}{1.54} = 2.95$	$\Delta T\|_{Si/SiC} = \frac{330-300}{310-300} = 3$
$\Delta K\|_{Si/Sapphire} = \frac{1.54}{0.35} = 4.4$	$\Delta T\|_{Sapphire/Si} = \frac{422-300}{330-300} = 4.06$
$\Delta K\|_{SiC/Sapphire} = \frac{4.55}{0.35} = 13$	$\Delta T\|_{Sapphire/SiC} = \frac{422-300}{310-300} = 12.2$

In 3D-TCAD thermal simulations, the thermal resistance is extracted by dividing the increment in lattice temperature by the total power applied across the heat source. In order to validate the simulation results, R_{TH} extracted from pulsed I-V measurements are compared with simulation results. The comparison of the simulated and measured thermal resistances are

shown in Fig. 5.13 (a). An excellent agreement is achieved between the measured and simulated thermal resistances for various geometries of the devices and using different substrates. However, it is important to note that there is no significant difference observed in obtained R_{TH} values of AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrates. This is due to the lower thermal conductivity of the AlGaN buffer used in these devices [5.16]. The simulated thermal resistance as a function of gate length for various device geometries grown on Si and SiC substrate is shown in Fig. 5.13 (b).



(a) (b)

Fig. 5.13. (a) Comparison of extracted R_{TH} as a function of device width, W_G between measurements and TCAD simulations for the AlN/GaN/AlGaN HEMT devices grown on different substrates (b) Extracted R_{TH} as a function of gate length, L_G and for various geometries of device.

5.7. Thermal Modeling Using Electro-Thermal Networks

5.7.1. Electrical Representation of Thermal Systems

In general, the propagation of heat in any system occurs via three different ways, i.e. convection, heat radiation or conduction. However, for electronic systems, the heat propagation take place essentially through heat conduction which is described by a partial differential equation for the case of homogeneous isotropic medium [5.10]:

$$\frac{\partial^2 T}{\partial x^2} = \frac{c.\rho}{\kappa} . \frac{\partial T}{\partial t} \qquad (5.14)$$

Where c is the specific thermal capacitance, ρ is the density of the material, κ is the specific heat conductance, T is the temperature and x represent the co-ordinates in the direction of heat propagation.

The electrical analog model for heat conduction can be the transmission line model, although its physical properties are described by a complex equation [5.10]:

$$\frac{\partial^2 U}{\partial x^2} = C'.L'.\frac{\partial^2 U}{\partial t^2} + \left(C'.R' + G'.L'\right)\frac{\partial U}{\partial t} + G'.R'.U \tag{5.15}$$

Where C', R', G' and L' are the capacitance, resistance, conductance and inductance per unit length, respectively.

The equations (5.14) and (5.15) describes two different physical process and hence they have no direct physical relationship between them. However, if we consider the fact that, the heat conduction in solid media, there is no equivalent term for the electrical parameters of inductance and such that a volume element cannot cool itself. This can be described using L'= G'=0 and therefore, the transmission line equation can be reduced to [5.10]:

$$\frac{\partial^2 U}{\partial x^2} = C'.R'\frac{\partial U}{\partial t} \tag{5.16}$$

Therefore, equations (5.14) and (5.16) can have the same form. Moreover, Kirchhoff stated that "two different forms of energy behave identically when the basic differential equations which describe them have the same form and the initial and boundary conditions are identical [5.11]". According to equations (5.14) and (5.16), the process of heat conduction can be therefore modeled using a transmission line equivalent circuit consisting of R and C elements only. The analogy between electrical and the thermal parameters are given in Table 5.3 and the electrical transmission line equivalent circuit diagram for modeling heat conduction process is shown in Fig. 5.14.

Table 5.3. Analogy between thermal and electrical parameters.

Thermal	**Electrical**
Temperature (T in K)	Voltage (U in V)
Heat Flow (P in W)	Current (I in A)
Thermal Resistance (R_{TH} in K/W)	Resistance (R in V/A)
Thermal Capacitance (C_{TH} in W.s/K)	Capacitance (C in A.s/V)

5.7.2. Electro-thermal Network Topologies

The thermal network representing the complete layout of the device tend to be very large, therefore it increases the complexity of modeling, increasing the simulation time and leading to numerical convergence issues. However, this would provide extensive information on temperature parameter in various regions of the device. Nowadays, the most widely used modeling approach in commercial electro-thermal simulators is to use mono-dimensional networks [5.11], in specific, a single RC network is used to model thermal behavior using the junction temperature and the dissipated power in the device. Some of the widely used electro-thermal network topologies are explained in this section.

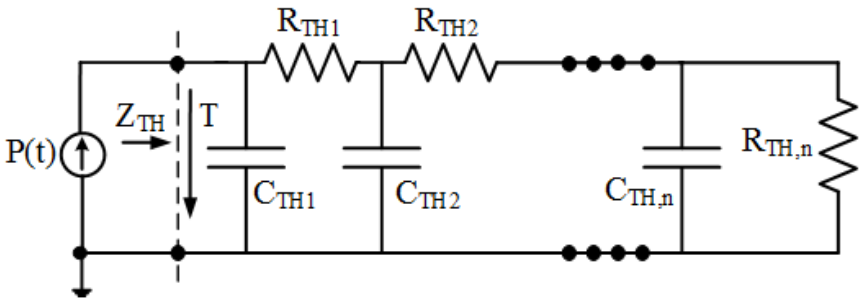


Fig. 5.14. Electrical transmission line equivalent circuit for modeling thermal conduction.

The rise in device temperature due to self-heating effect is represented using a single pole electro-thermal equivalent network [5.14] as shown in Fig. 5.15.

The thermal impedance in Laplace domain is given by the following equation [5.14]:

$$Z_{TH}(p) = \frac{R_{TH}}{1 + pR_{TH}C_{TH}} \tag{5.17}$$

Where *p* is the Laplace variable.

The first order self-heating model can be given by the dynamic relationship between instantaneous power dissipation ($P_{diss}(t)$) and the rise in device temperature [5.14]:

$$T_{rise}(t) = \Delta T\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) \tag{5.18}$$

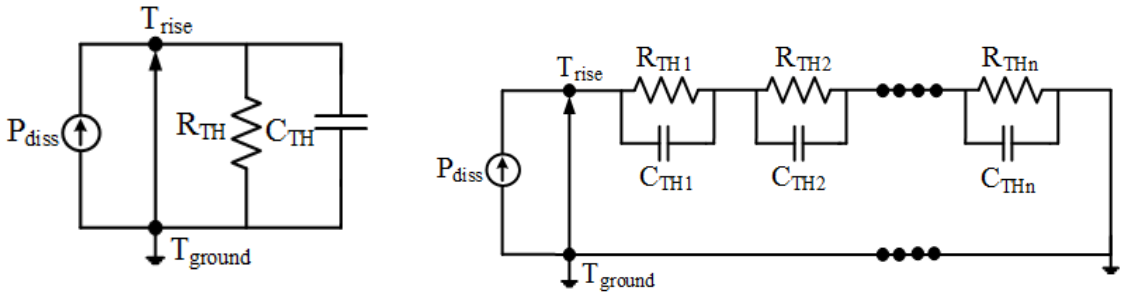
Where $\Delta T = P_{diss}(t).R_{TH}$ is the magnitude of the temperature step and $\tau = R_{TH}.C_{TH}$ is the time constant.

The model shown in Fig. 5.15 (a) is the reduced form of the generalized thermal equivalent circuit (Foster network) shown in Fig. 5.15 (b). In general, the diffusion process in the medium

is described as the superposition of infinite number of modes. Moreover, each mode can be characterized by its Eigen function and its associated time constant τ_i. Therefore, the precise solution of the heat transform problem can be expressed using the following form [5.14]:

$$T_{rise}(t) = \sum_{i=1}^{n} \Delta T_i \left(1 - \exp\left(-\frac{t}{\tau_i}\right)\right) \tag{5.19}$$

Where $\Delta T_i = P_{diss}(t).R_{THi}$ and $\tau_i = R_{THi}.C_{THi}$.



(a) (b)

Fig. 5.15. (a) A single pole electro-thermal network (b) Foster network – generalized thermal equivalent circuit.

The Foster Network

The Foster network shown in Fig. 5.15 (b) is based on infinite set of exponential time constants equivalent to a step response with zero initial conditions. Each time constant is simply equal to the product of the resistance and the capacitance of each cell in the network. Typically, four time constants are adequate to describe the thermal impedance of the system with sufficient accuracy. Therefore, the transfer function of a Foster network in time domain, by [5.11]:

$$Z_{TH}(t) = \sum_{i=1}^{n} R_{THi} \left(1 - \exp\left(-\frac{t}{\tau_i}\right)\right) \tag{5.20}$$

and in frequency domain by [5.11]:

$$Z_{TH}(f) = \sum_{i=1}^{n} \frac{R_{THi}}{1 + j.2\pi.f.\tau_i} \tag{5.21}$$

The transfer function using Laplace network to the response of the network in time domain is given by [5.14]:

$$Z_{TH}(p) = \sum_{i=1}^{n} \frac{R_{THi}}{1 + pR_{THi}C_{THi}} \tag{5.22}$$

The Foster network is very simple to implement, however it can be used to describe only the thermal behavior at the input node and therefore, the internal nodes do not have a physical

meaning. In fact, changing the order of RC cells in the Foster model does not affect the overall response of the system and this indicates that there is no physical relation between the device structure and an individual RC cell. Moreover, this network cannot be used to determine the temperature distribution within the device.

The Cauer Network

The Cauer network is more convenient way to describe physically the thermal behavior of the system. The element values of the Cauer networks can be determined by employing the heat equation [5.14]. Unlike the Foster network, the Cauer network can describe the internal temperature distribution of the system since the thermal capacitances are connected to thermal references (electrical or thermal ground). Moreover, each cell of the Cauer network is the physical representation of heat-conducting structure layers and therefore, each cell can contribute to the total thermal impedance of the system.

In contrast to Foster network, there is no direct relation between time constants τ_i and thermal parameters (R_{THi} and C_{THi}) for Cauer network shown in Fig. 5.16. Indeed, the time constant of each cell depends on all the thermal parameters of the system, leading to a complex mathematical representation of the system. The transfer function of the Cauer network using Laplace transforms can be expressed as [5.11]:

$$Z_{TH}(p) = Z_{TH1}(p) + \cfrac{1}{Y_{TH1}(p) + \cfrac{1}{Z_{TH2}(p) + \cfrac{1}{Y_{TH2}(p) + 1/\ldots}}} \tag{5.23}$$

Where Z_{THi} *(p)* and Y_{THi} *(p)* are the thermal impedance and admittance of the i-th cell in the Cauer network.

The Cauer network can be transformed to the equivalent Foster network and vice versa using the conventional circuit transformation principle [5.11].

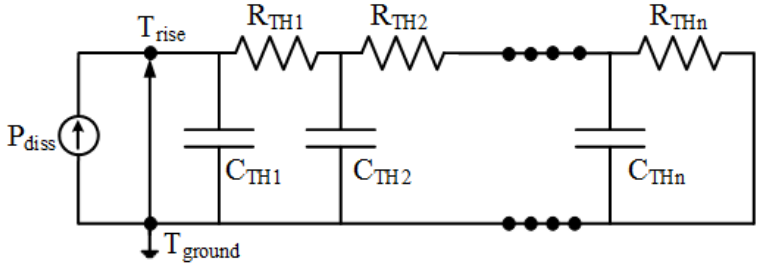


Fig. 5.16. Electro-thermal Cauer network.

Modified Recursive Network

It is basically a Cauer type network where the RC elements are placed in recursive order. The recursive network treats that every element is a heat generating sphere [5.14]. Therefore, the time-dependent heat diffusion can be modeled using the circuit shown in Fig. 5.17 where the respective thermal resistance element decreases and the capacitance element increases and these have been modeled using different recursive factors, K_r (<1)and K_c (>1), for resistance and capacitance, respectively. The transient variation of device temperature is modeled by C_{TH}, however, under steady-state conditions, C_{TH} has no physical meaning [5.8]. Therefore, the thermal resistance can be expressed as the sum of resistances of each recursive cell existing in the circuit. It is worth to note that, higher the number of cells may provide better accuracy, however it suffers from large simulation time.

The thermal resistance of the modified recursive network under steady-state conditions can be expressed using [5.8]:

$$R_{TH} = \sum_{n=0}^{N} K_{ri}^{n}.R \tag{5.24}$$

i = 1,2, … m.

Where N represent the number of cells in the recursive network.

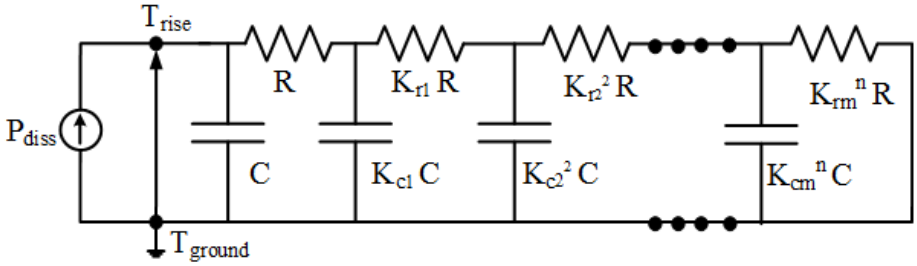


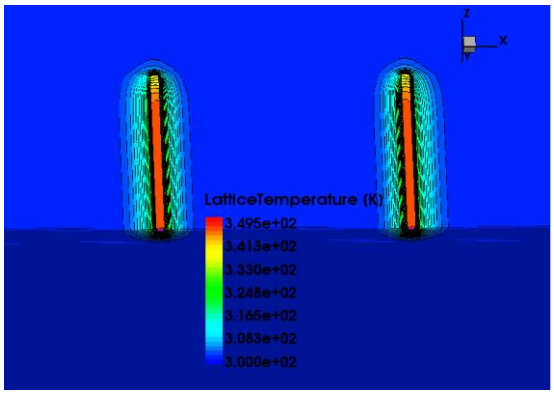
Fig. 5.17. Modified recursive network.

5.7.3. Transient Thermal Simulation and Modeling

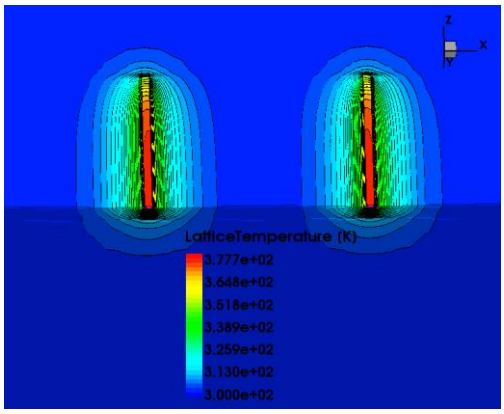
In order to obtain the variation of device temperature with time, large signal thermal simulations have been performed by applying an electric pulse (P_{pulse}) at the heat source of the device. The square wave pulse is used and the following pulse conditions are applied: delay time (t_d) = 40 ns, rise time (t_r) = 10 ns, fall time (t_f) = 10 ns, pulse width (t_{pw}) = 15 µs and pulse period (t_{pp}) = 20 µs. The simulations have been performed for different input power applied at the heat source and for different device geometries of the devices grown on Si and SiC substrate. The lattice temperature ($T_{Lattice}$) distribution inside the 2×25µm AlN/GaN/AlGaN HEMT grown on Si

HEMT for different transient pulse times is shown in Fig. 5.18. This demonstrates that lattice temperature increases gradually with increasing pulse time. Moreover, the transient variation of device temperature (ΔT_j) has been modeled using the modified recursive network shown in Fig. 5.17. The obtained results for various device geometries of the devices grown on Si and SiC substrate are given in this section.

When the transient power is applied to the heat source of the device, theoretically an infinite number of thermal time constants are required to describe the thermal behavior of the complete device structure, which is generally composed of several materials.



(a)



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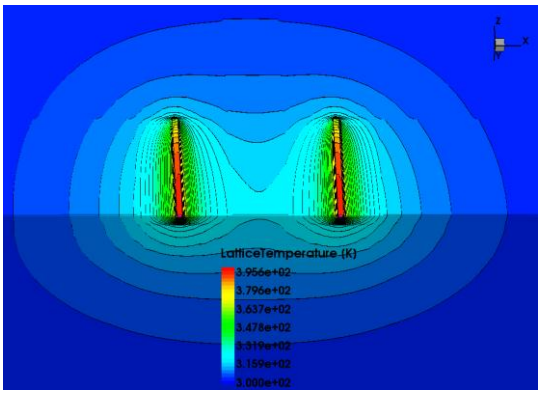

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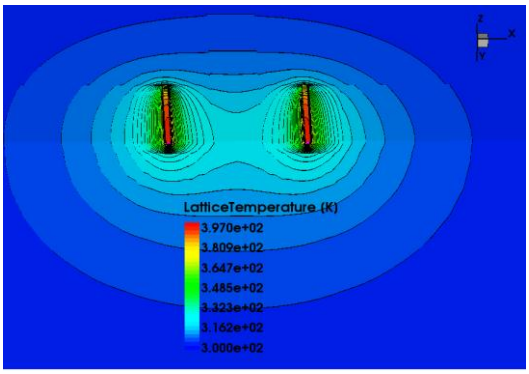

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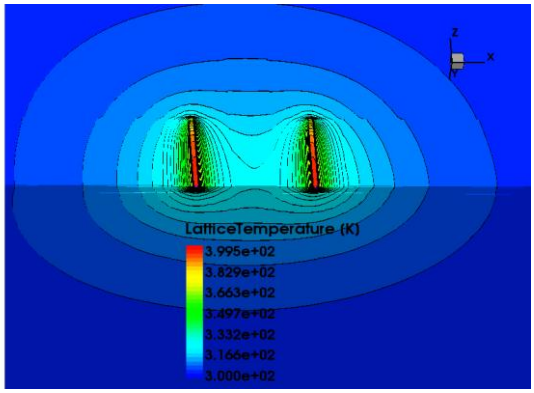

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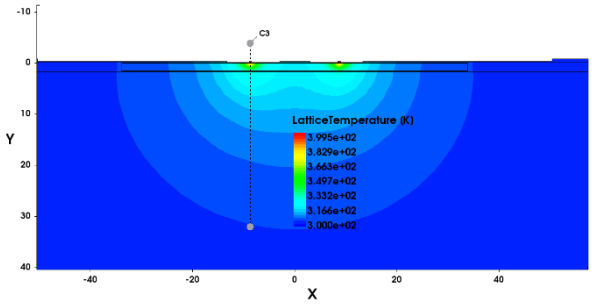
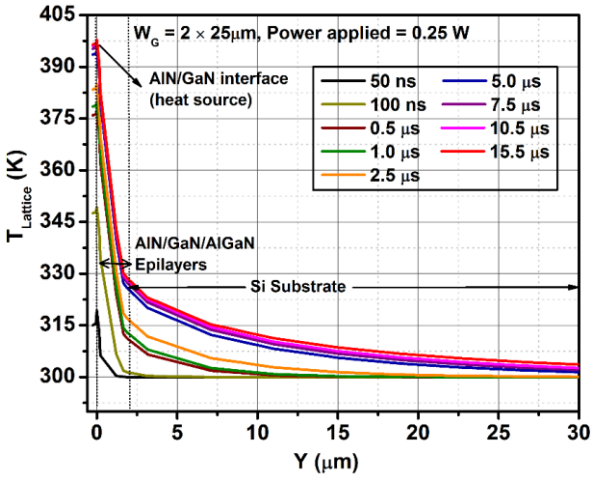


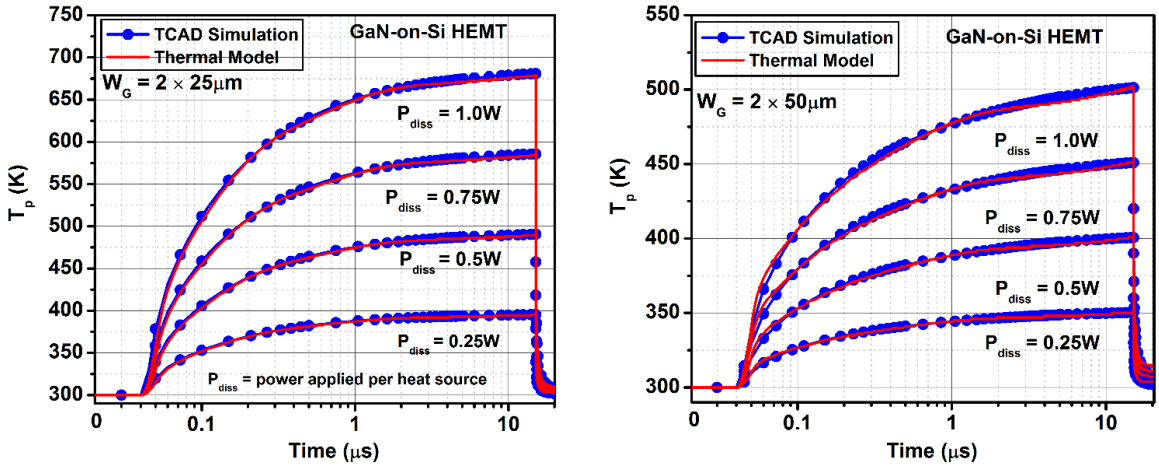
(f)



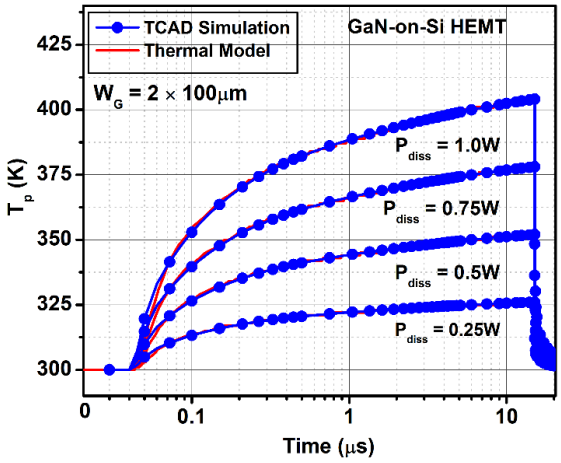
(g)

Fig. 5.18. Lattice temperature distribution at different transient conditions for the applied power of 0.125 W per heat source of AlN/GaN/AlGaN HEMT grown on Si substrate and with device width, W_G = 2×25 µm. (a) 100 ns (b) 500 ns (c) 5.0 µs (d) 7.5 µs (e) 15.5 µs (f) 2D-view showing the variation of lattice temperature at transient time = 15.5 µs and (g) Lattice temperature variation along the transverse direction (Y) through the middle of heat source and for different simulation transient times.

Therefore, the dynamic self-heating response of the device could not be modeled properly with a traditional single-pole network, since it is associated only with a single time constant [5.8]. Therefore, we have considered the modified recursive network shown in Fig. 5.17 for modeling the transient behavior of the device. Moreover, increasing the number of cells in the recursive network improves the accuracy, both in time and frequency domain. For our modeling, five cells have been considered to provide better accuracy.



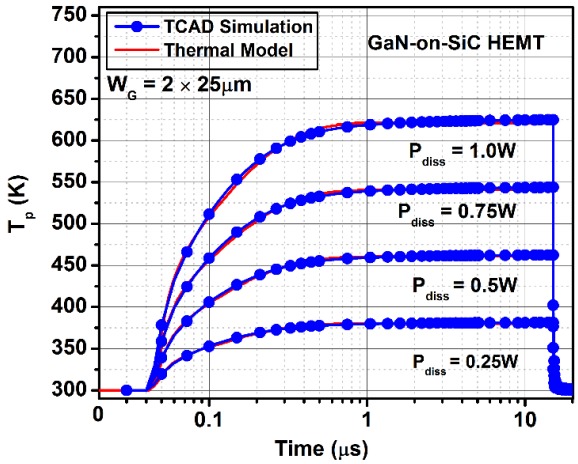
(a) (b)



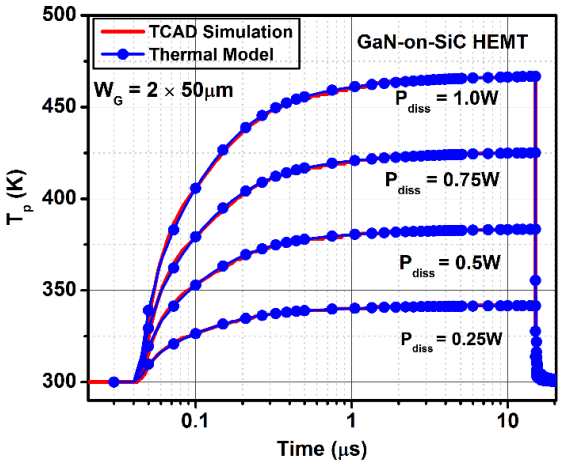
(c)

Fig. 5.19. 3D-TCAD thermal simulation and recursive thermal modeling of AlN/GaN/AlGaN HEMTs grown on Si substrate. (a) 2×25µm (b) 2×50µm and (c) 2×100µm.

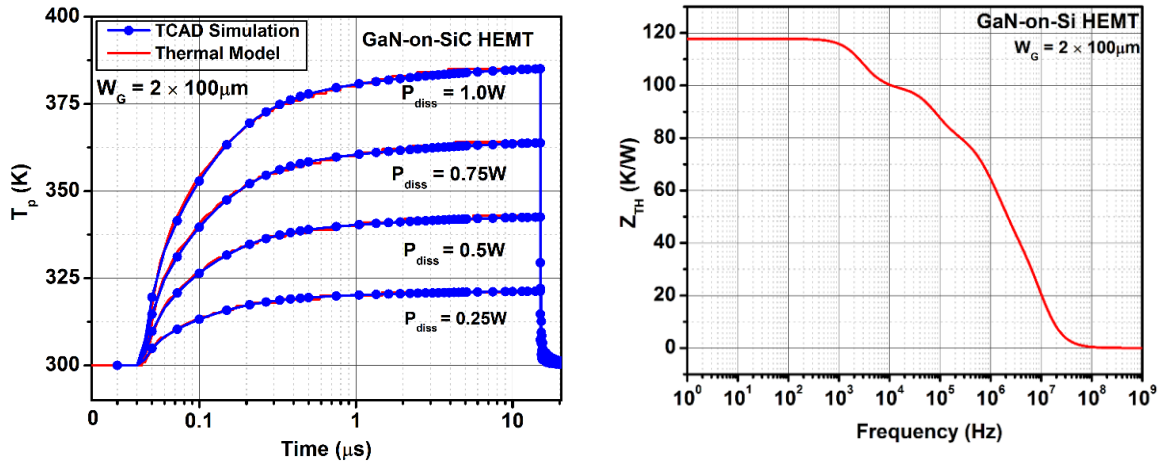
The simulations have been performed for different dissipated power applied at the heat source of the device and this corresponds to different power density generated inside the device. The corresponding observed increase in transient temperature has been modeled using the modified recursive network. Fig. 5.19 and 5.20 show the comparison of 3D-TCAD thermal simulation and thermal modeling results of the AlN/GaN/HEMT devices grown on Si and SiC substrates, for various device geometries. An excellent agreement is achieved between the TCAD thermal simulation and recursive model for various geometries of the device. The simulated thermal impedance (Z_{TH}) for 2×100µm AlN/GaN/AlGaN HEMT grown on Si substrate as a function of frequency using recursive thermal model is shown in Fig. 5.20 (d). It is worth a while to note that atleast three time constants are clearly observable in the simulated characteristics and this can be related to the different material layers existing in the device.



(a)



(b)



(c) (d)

Fig. 5.20. 3D-TCAD thermal simulation and recursive thermal modeling of AlN/GaN/AlGaN HEMTs grown on SiC substrate. (a) 2×25µm (b) 2×50µm and (c) 2×100µm (d) Simulated thermal impedance of 2×100µm device grown on Si substrate using recursive thermal network.

5.8. Summary

In this chapter, we first extracted the thermal resistance of AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrates through on-wafer pulsed I-V measurements. Then, we studied the thermal behavior of the same AlN/GaN/HEMT devices grown on different substrates through 3D-TCAD thermal simulations. The thermal resistances extracted for various geometries of the devices using TCAD thermal simulations are compared with measurements and found to be in excellent agreement. Then, we investigated the thermal behavior of these devices by applying the transient pulse across the heat source of the device. The obtained transient thermal characteristics of the devices are modeled using the modified recursive network and an excellent agreement is obtained between TCAD simulations and the recursive thermal model. This will ease the circuit designers to integrate the thermal model while developing the large signal model (LSM) of device.

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Conclusions and Scope of Future Works

Conclusions

GaN HEMT device technology demonstrates a great deal of potential for all high frequency and high power microwave and RF applications which pushes the limits of conventional Si or GaAs based devices. However, these GaN HEMT devices are considered to be relatively immature due to the existence of defects/traps in the device which significantly degrade their performance. The presence of traps in the device causes different degradation mechanisms such as current collapse, transconductace dispersion, admittance dispersion, gate-lag, drain-lag, increased gate leakage and low frequency noise. The focus of this thesis work is to characterize the different aspects of GaN/AlGaN/GaN HEMT and AlN/GaN HEMT device technology using experimental characterization and TCAD-based physical device simulations. The research work presented in this thesis would benefit other members of the GaN HEMT community in order to completely understand the trapping mechanisms, particularly buffer related trapping effects, and also other important characteristics such as on-resistance (R_{ON}) and thermal-resistance (R_{TH}) of these GaN HEMT devices. Moreover, this research study could also provide an efficient feedback for further improving the GaN HEMT device technology and its respective RF performance.

Chapter 1 discussed the potential of GaN material in comparison with other semiconductor materials which makes them as an extremely powerful candidate for high power microwave and mm-wave applications. The brief history of evolution of GaN-based HEMT devices and the technological developments reported over the years, and the corresponding obtained improved device performances have been described in detail. Moreover, the performance of conventional AlGaN/GaN HEMT devices have been limited by the use of ultra-short gate lengths and ultra-thin AlGaN barrier. This give rise to AlN/GaN HEMT devices and also considered to be a suitable alternative to replace AlGaN/GaN HEMT devices. The polarization mechanisms and the theory of device operation, implementation of field-plates to improve the RF performance have been explained. Furthermore, the degradation mechanisms of GaN HEMTs such as current collapse, gate-lag, drain-lag, self-heating, and gate-edge degradation have been illustrated with the aid of theoretical diagrams. Although the scope of this thesis work is not to characterize the gate leakage mechanisms of GaN HEMT devices, it is however essential to understand the influence of gate leakage on device performance. The different tunneling mechanisms used to characterize the gate leakage have been described.

Chapter 2 presented the physics based analytical modeling of current-voltage characteristics of AlGaN/GaN HEMT devices. The theoretical method used for estimating the Al-mole fraction (m) dependent polarization charges and the necessary analytical equations have been provided. A simple analytical model for estimating the sheet carrier density (n_s) has been explained. The analytically calculated sheet carrier density as a function of gate voltage (V_{GS}) and Al-mole fraction (m), are validated using our numerical simulation results. Then, a simple analytical model valid for calculating both intrinsic and extrinsic current-voltage characteristics of AlGaN HEMT device has been presented. The intrinsic HEMT model characteristics have been verified using TCAD simulation results, and an excellent agreement is achieved between analytical model and TCAD simulation. The extrinsic HEMT device characteristics have been validated using experimental results reported in the literature and in-house measured device characteristics. For long channel devices with different device dimensions, the proposed analytical model achieves a reasonable agreement with experimental characteristics. However for short channel device, the proposed model results show a large discrepancies with in-house measured characteristics. This is due to the proposed model does not consider short channel effects and channel length modulation which has large influence on the performance of submicron gate length devices.

The second part of the chapter 2 describes the TCAD Sentaurus simulation methodology used in this thesis work. A brief overview of the TCAD Sentaurus simulation platform, with a brief description of the simulation tools utilized and different kinds of simulation models available has been provided. The basic theory of the formation of two dimensional electron gas (2DEG) sheet density in AlGaN/GaN heterostructure has been explained using theoretical diagrams and TCAD simulations. It is clear from the simulation results, for the case of ideal surface and when the AlGaN barrier thickness (d) is less than critical thickness (d_{CR}), there is no 2DEG channel formation occurs at the AlGaN/GaN hetero-junction interface. However, the increase in AlGaN barrier thickness, $d > d_{CR}$, causes the accumulation of electrons at the AlGaN/GaN interface and the corresponding holes are accumulated at the surface**.** This simulation study proves the theoretical fact that for the case of ideal surface, the 2DEG sheet density is formed only due to the accumulation of holes at the surface of the device. Furthermore, the influence of donor density and energy level in the formation of 2DEG sheet density have been studied. The three regions have been identified as the surface donor density and its associated energy level are varied. In Region 1, the surface donor density has negligible influence on the 2DEG sheet density whereas in Region 2, the 2DEG sheet density increases linearly with donor density and

is independent of the energy level. However, in Region 3, the surface donor's energy level has a strong influence on 2DEG sheet density and the donor density has negligible influence. The comparison of different kinds of simulation model have been explained. Moreover, the drift-diffusion (DD) and hydrodynamic (HD) model achieves the same result at lower gate biases. This thesis work is primarily focused on characterizing the devices under class AB operation as this mode of operation is widely preferred for designing RF power amplifiers. Therefore, the simulation result suggested that DD model is sufficient for all our analysis and therefore, DD model is used for rest of the TCAD simulation results presented in this thesis.

Chapter 3 investigates the trapping mechanisms of GaN/AlGaN/GaN HEMT transistors using experimental characterization and TCAD-based physical simulations. The different types of device characterization techniques such as pulsed *I-V*, LF-S parameters and LF noise bench have been described. The LF S-parameters measurement has been performed on 8×75µm device under deep class-AB operation mode and the measured S-parameters are converted into their equivalent Y-parameters. The traps existing in the GaN buffer cause the frequency dispersion in the output admittance Y_{22} parameter. Moreover, the emission time constant (τ_n) changes with measurement temperature and therefore, the emission time constant is calculated at each temperature and then by using Arrhenius law, the apparent activation energy (E_a) and apparent cross section of traps (σ_n) have been determined. The thermal resistance (R_{TH}) of the device has been found to be 20.42 °C/W and used in the extraction of trap parameters. The extracted activation energy and cross section of the traps are 0.4 eV below the conduction band and 1.89×10^{-16} cm^2, respectively. In order to understand the physical origin of this traps, a comprehensive analysis of the traps reported in the literature has been studied. This study suggested that the origin of this traps could be related to the iron doping present in the GaN buffer. However, in order to understand the physical location of traps, two-dimensional TCAD physical simulations have been used. In order to make physical simulations meaningful, it is essential to calibrate the TCAD simulation model in order to reproduce the measured data. The calibration process of TCAD simulation model has been explained. The simulation model has been calibrated for both 8×75 and 6×75-µm devices respectively, and are used for rest of the analysis presented in this chapter. Using the calibrated TCAD simulation model, LF admittance Y_{22} parameter simulation has been carried out using the same measurement biasing conditions. The junction temperature (T_j) has been estimated based on the known values of R_{TH}, T_{chuck} and power dissipation (P_{diss}), and are used in simulations. Moreover, the acceptor traps concentration (N_{TA}) of 5.0×10^{16} cm^3 and σ_n value of 3.2×10^{-18} cm^2 has been used. A good

agreement between the TCAD simulations and measurement Y_{22} parameter confirms the existence of acceptor-like traps in the GaN buffer. To the best of our knowledge, this is the first time that such a comparison between the physical simulation and measurement parameter has been reported for the GaN HEMT technology. Moreover, if the donor traps are existing in the GaN buffer, the simulated Y_{22} parameter does not show the frequency shift as the temperature increases, instead the peak amplitude increases with temperature. This type of behavior has been observed in our AlN/GaN HEMT devices. Therefore, we suggest that LF admittance measurement is an effective tool for characterizing the traps present in the GaN buffer. In case, if the traps are existing in the AlGaN barrier, this particular measurement technique could not be useful for detecting the traps and this has been validated using our TCAD simulations. Then, LF noise measurements has been carried out on 6×75µm device and the respective traps physical properties such as E_a and σ_n of the device have been extracted. Two traps have been identified and the apparent activation energies of the traps determined are 0.57 and 0.51 eV, respectively. The corresponding cross sections determined are 2.13×10^{-16} and 4.96×10^{-15} cm^2, respectively. The extracted activation energies of these traps are in excellent agreement with the Fe-doped GaN HEMT devices. In order to physically confirm the location of these traps, TCAD simulations have been carried out by including these traps in the GaN buffer close to the GaN channel region. The total GaN buffer is divided into three regions and these two traps are introduced in the first two regions of GaN buffer. T2 with an activation energy of 0.51 eV are introduced in the first region and T1 having E_a of 0.57 eV are introduced in the second region of the GaN buffer, respectively. A good agreement has been achieved between TCAD simulation and measurement drain noise spectral density physically confirms that these two traps are located in the GaN buffer. This is the first time that such a comparison of noise characteristics has been reported for GaN HEMT devices. Moreover, it is concluded from the simulation results, T1 related dispersion in the noise characteristics occurs at very low frequencies and hence this trap is clearly visible only at higher operating temperatures. Furthermore, this study also suggest that low frequency noise measurement is another effective tool for characterizing the traps existing in the GaN buffer. The time-domain drain-lag characterization has been performed on 6×75µm device and the measured transient drain current characteristics shows a slow recovery of drain current with a relative long time constant, confirms the existence of traps in the device. The TCAD transient simulation result concludes that traps existing in the GaN buffer are responsible for the drain-lag phenomenon observed in measurement. Therefore, the simulation results presented in this chapter establish a correlation

with measurements in order to identify the physical location of traps in the device and also very useful to validate the measurement methodology.

The first part of the chapter 4 investigates the influence of GaN channel traps on the performance of AlN/GaN/AlGaN HEMT device through two-dimensional TCAD numerical simulations. The physical properties of the traps used in the study have been taken from the literature data. The TCAD simulation model is calibrated for 2×100µm device using the experimentally measured dc I-V characteristics. A good agreement has been achieved between the TCAD simulation and measured I-V characteristics confirms the validity of the calibrated physical model. The calibrated simulation model is used for analyzing the device characteristics by including different types of traps in the GaN channel. The simulation results demonstrate that acceptor-like traps whose energy level lies deep inside the conduction band causes a significant reduction of drain current and also the shift of pinch-off voltage of the device. However, the donor-like traps gets ionized only at high negative gate biasing and only for shallow trap energy level lies inside the conduction band. Therefore, it can be concluded that acceptor-like traps have a significant influence on the simulated dc I-V characteristics whereas the donor-like traps have no considerable influence. Moreover, the simulation results also suggest that deeper the energy level of acceptor-like traps, more the possibility of ionization of these traps and hence, larger the reduction in drain current performance of the device.

In the second part of chapter 4, we first studied the temperature dependency of on-resistance (R_{ON}) of AlN/GaN/AlGaN HEMT devices grown on SiC substrate through dc and low-frequency S-parameters measurements. The R_{ON} has been extracted from the dc I-V and LF S-parameters measurements for various device geometries of the devices grown on SiC substrate. A good agreement has been obtained between the two methods demonstrate that the proposed extraction procedure remains valid for various geometries of the device. Moreover, using the calibrated 2×100µm device simulation model, the R_{ON} has been simulated for various operating device temperature. A good agreement has been observed between the measurement and TCAD simulation over the temperature range of 0ºC to 150ºC. Then, we have proposed a simple methodology for extracting the temperature dependence of channel sheet resistance (R_{sh}) and parasitic series contact resistance (R_{se}) of the device technology. The detailed procedure for extracting sheet resistance and contact resistance has been illustrated with the aid of flowchart. The proposed methodology has been applied on 2×50µm device low frequency measurement data with different gate-drain distances (L_{GD}) of 1.0, 2.0 and 3.0 µm, respectively. The corresponding R_{sh} and R_{se} have been extracted as a function of gate bias voltages and operating

device temperature. Moreover, the extracted value of sheet resistance is in agreement with the already reported value of this device technology. The proposed extraction procedure has also been verified using TCAD device simulations. The variation observed in the extracted R_{sh} and R_{se} between measurements and TCAD simulations are only due to the calibration error, because the 2×100µm device calibrated parameters have been used for 2×50µm device simulations. Therefore, it can be concluded that this proposed methodology can be applied to any device technology in order to extract the channel sheet resistance and parasitic contact resistances.

Chapter 5 investigates the thermal behavior of AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrates through on-wafer pulsed I-V measurements and three-dimensional (3D) TCAD-based thermal simulations. The thermal resistances have been extracted for various device geometries using measurements and TCAD thermal simulations and found to be in excellent agreement. In thermal simulations, the external heat source is assumed and the generated heat is applied at the heat source, which then dissipates the heat into the device structure obeying the heat flow mechanism. The length of the heat source (L_{HS}) is optimized in order to achieve a match between the simulated and experimentally measured thermal resistance. A good match is obtained when the L_{HS} is chosen to be twice the gate length of the device and this implies that hot spot is located at the drain-side gate edge. Then, we have investigated the thermal behavior by applying the transient pulse at the heat source of the device. The obtained transient thermal characteristics have been modeled using modified recursive network and an excellent agreement is achieved between TCAD simulations and thermal model, for various device geometries of the devices grown on Si and SiC substrates. Therefore, the developed thermal model will be handful for circuit designers to integrate this thermal model while developing the large signal model (LSM) of the device.

Scope of Future Works

A number of possible improvements can be added to the work presented in this thesis in order to completely understand the degradation mechanisms of GaN HEMT device technology. This would benefit both the device fabrication individuals and RF circuit designer's community to gain the knowledge on physical degradation mechanisms and its impact on device/circuit performance. The possible scopes of future works are summarized below:

(1) Extension of physics-based analytical modeling

The analytical drain current model presented in this thesis is capable of predicting the extrinsic HEMT characteristics of the device with reasonable accuracy for the case of long channel devices. However, the proposed model does not include some physical effects like channel length modulation, self-heating, short channel effect and mobility degradation. These physical effects must be included into the developed model in order to accurately predict the device characteristics, especially for sub-micron gate length devices. Moreover, the existence of traps in the GaN HEMTs significantly influence the device characteristics. Therefore, the trapping effects need to be incorporated into the physical model. Then, the developed physical model can be integrated with the modern circuit simulators and this would greatly benefit the circuit designers to predict the device performance for high frequency and high power applications.

(2) Characterization of Barrier Traps

In the chapter 3 of this thesis, we attempt to characterize the traps existing in the GaN buffer region of the device using different measurement techniques and TCAD physical simulations. However, the traps may also exist in the AlGaN barrier of the device structure. Therefore, it is essential to characterize the barrier traps and also to understand their influence on device performance. The following two possible ways could be useful for characterizing the barrier traps: (1) performing the LF input gate noise measurements of the device at various operating temperatures and this would allow to identify the type of traps and their corresponding physical properties such as activation energy (E_a) and cross section (σ_n). (2) performing I-DLTS measurement of the device by pulsing the gate bias voltage well below pinch-off to ON state and at fixed drain potential. This would allow to extract the time constant of traps and therefore, repeating this measurement at different temperatures, and then by using Arrhenius equation, the physical properties of traps can be determined. Then, by using TCAD physical simulations it is possible to physically confirm the location of traps in the device.

(3) Gate Leakage Characterization

Gate leakage becomes significantly important in determining the power dissipation and reliability of these devices. Moreover, for the case of AlN/GaN HEMT devices, the barrier layer is very thin and this causes the high electric field across the barrier and this results in increased electrons tunneling through the barrier, leading to larger gate leakage current. Therefore, it is important to measure the gate leakage characteristics of these devices. Moreover, using TCAD physical simulations, it is crucial to understand the leakage current mechanisms of the device over a wide range of bias and temperature. Indeed, TCAD physical simulations would help to identify the type of leakage mechanisms (Poole-Frenkel emission, Fowler-Nordheim tunneling or Trap-Assisted-Tunneling) occurring in the device. Furthermore, it is also helpful to examine the impact of AlGaN barrier traps on the gate leakage performance of the device.

(4) Poole-Frenkel Assisted Traps Emission

The emission rate of traps is not only dependent on temperature but also strongly dependent on applied drain biasing (electric field in the device). Therefore, it would be useful to analyze the bias dependent admittance characteristics.

(5) Electro-thermal Simulations

In the thermal simulations of AlN/GaN/AlGaN HEMT devices presented in chapter 5, we assumed an external heat source to dissipate the required heat into the device structure. The width of the heat source is assumed to be the gate width and the length of the heat source is optimized in order to achieve a good match between the simulated and measured thermal resistance. Therefore, the simulations performed are purely thermal. However, TCAD simulation tool is capable of solving self-consistently the basic Poisson's equation along with the lattice heat flow equation to generate the heat dissipation inside the device. This would automatically compute the heat dissipation area (hot spot) accordingly and eliminates the need of assumption of an external heat source and the associated optimization process. Indeed, the simulation will be purely electro-thermal and could offer better understanding of device characteristics.

(6) Large Signal Model (LSM)

The development of LSM including trapping mechanisms, low frequency noise sources and thermal effects would significantly benefit the RF designer's community.

List of Publications

Publications

International Journals: 6

1. A. K. Sahoo, **N. K. Subramani**, J-C. Nallatamby, L. Sylvain, C. Loyez, R. Quéré and F. Medjdoub, "Small Signal Modeling of High Electron Mobility Transistors on Silicon and Silicon Carbide Substrate with Consideration of Substrate Loss", *Solid State Electronics*, vol. 115, pp: 12 - 16, Jan. 2016.

2. **Nandha Kumar Subramani**, Amit Kumar Sahoo, Jean-Christophe Nallatamby, Raphael Sommet, Nathalie Rolland, Farid Medjdoub and Raymond Quéré, "Characterization of Parasitic Resistances of AlN/GaN/AlGaN HEMTs through TCAD-Based Device Simulations and On-Wafer Measurements", *IEEE Trans. on Microwave Theory and Techniques*, vol. 64, pp: 1351 – 1358, May 2016.

3. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby, Raphael Sommet and Raymond Quéré, "Identification of GaN Buffer Traps in Microwave Power of AlGaN/GaN HEMTs through Low Frequency S-Parameters Measurements and TCAD-Based Physical Device Simulations", *IEEE Journal of the Electron Devices Society*, vol. 5, pp: 175 – 181, May 2017.

4. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby, Michel Prigent and Raymond Quéré, " Low Frequency Noise Characterization in GaN HEMTs: Investigation of deep levels and their physical properties", *IEEE Electron Device Letters*, vol. 38, pp: 1109 – 1112, Aug. 2017.

5. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby and Raymond Quéré, "Low Frequency Drain Noise Characterization and TCAD Physical Device Simulations: Identification and analysis of GaN buffer traps", *IEEE Electron Device Letters*, in press, Nov. 2017.

6. **Nandha Kumar Subramani**, Julien Couvidat, Ahmad Al Hajjar, Jean-Christophe Nallatamby and Raymond Quéré, "Drain-Lag Characterization and TCAD-based Device Simulations of GaN HEMTs: Identification of physical location of traps causing drain-lag effects", *IEEE Trans. on Electron Devices*, in preparation, Oct. 2017.

International Conferences: 4

1**.** A. K. Sahoo, **N. K. Subramani**, J-C. Nallatamby, N. Rolland, R. Quéré and F. Medjdoub, "Temperature Dependent Contact and Channel Sheet Resistance Extraction of GaN HEMT", *Integrated Nonlinear Microwave and Millimeter-wave Circuits Workshop (INMMIC)***,** pp: 1 **–** 3, Oct. 2015.

2. **N. K. Subramani**, A. K. Sahoo, J-C. Nallatamby, R. Sommet and R. Quéré, "Systematic Study of Traps in AlN/GaN/AlGaN HEMTs on SiC Substrate by Numerical TCAD Simulation", *12th Conference on PhD Research in Microelectronics and Electronics (PRIME)***,** pp: 1 **–** 4, June. 2016. Won: "Bronze Leaf Award".

3. A. K. Sahoo, **N. K. Subramani**, J-C. Nallatamby, R. Sommet, N. Rolland, R. Quéré and F. Medjdoub, " Thermal Analysis of AlN/GaN/AlGaN HEMTs grown on Si and SiC Substrate through TCAD Simulations and Measurements", *11th European Microwave Integrated Circuits Conference (EUMIC)***,** pp: 145 – 148, Oct. 2016.

4. **N. K. Subramani**, J-C. Nallatamby, B. Bindu, A. K. Sahoo, R. Sommet and R. Quéré, "A Physics Based Analytical Model and Numerical Simulation for Current-Voltage Characteristics of Microwave Power AlGaN/GaN HEMT ", *International Microwave and RF Conference (IMARC)***,** pp: 1 – 4, Dec. 2016.

National Conferences: 1

1. Julien Couvidat, **Nandha Kumar Subramani**, Ahmad Al Hajjar, Jean-Christophe Nallatamby, Raphael Sommet and Raymond Quéré, " Identification de piéges dans le buffer des HEMTs AlGaN/GaN basée sur des measures de paramétres S basse fréquence et sur des simulations physiques ", *Journées Nationales Microondes (JNM)*, May. 2017.

Appendix

Table A.I: Summary of the deep levels (traps) reported in the literature.

Reference	Activation Energy (eV)	Cross Section (cm^2)	Trap Concentration (cm^{-3})	Growth technique	Analyzed samples	Measurement Technique	Interpretation of traps
Fang [1]	0.06 – 0.07	$1 – 3 \times 10^{-20}$, $5 – 8 \times 10^{-19}$	-	MOCVD	n-type GaN (as-grown and electron irradiated)	DLTS	N-vacancy
Gassoumi [2]	0.06	2.1×10^{-15}	-	MBE	AlGaN/GaN/Si HEMT	Conductance DLTS	N-vacancy
Gassoumi [3]	0.07	2.65×10^{-15}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.22)	Conductance DLTS	N-vacancy
Gassoumi [2]	0.07	2.56×10^{-15}	-	MBE	AlGaN/GaN/Si HEMT	Conductance DLTS	GaN buffer
Umano-Membreno [4]	0.089	3.1×10^{-18}	2.8×10^{13}	MOCVD	Schottky diode on un-doped n-GaN (gamma irradiated)	Transient Capacitance Measurements	N-vacancy
Soh [5]	0.10	2.4×10^{-20}	1.3×10^{13}	MOCVD	Si-doped GaN	DLTS	Point defects such as N-vacancy
Chikhaoui [6]	0.12	1.8×10^{-18}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.24)	Fourier Transform DLTS	-
Chen [7]	0.125	9.6×10^{-17}	-	HVPE	n-GaN flims	DLTS	Electron beam irradiated induced defect

Sghaier [8]	0.13	1×10^{-18}	-	MOCVD	AlGaN/GaN/Al_2O_3 HEMT (Al =0.22)	Low Frequency Dispersion	Mg impurities
Umano-Membreno [4]	0.132	4.9×10^{-18}	2.5×10^{13}	MOCVD	Schottky diode on un-doped n-GaN (gamma irradiated)	Transient Capacitance Measurements	N-vacancy
Zhang [9]	0.14	3.6×10^{-15}	4.2×10^{14}	Ammonia MBE	n-type GaN (m-plane)	DLTS	-
Chung [10]	0.149	1.2×10^{-18}	8.97×10^{13}	MOVPE	Un-doped GaN flim	DLTS	Could be related to N-vacancy
Chikhaoui [6]	0.15	8.9×10^{-19}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.24)	Fourier Transform DLTS	Buffer/Interface states
Young [11]	0.15	2.0×10^{-18}	2.8×10^{16}	Plasma-assisted MBE	GaN/AlGaN/ Sapphire HEMT (Al =0.2)	DLTS	N-vacancy
Sghaier [8]	0.17	1.76×10^{-20}	-	MOCVD	AlGaN/GaN/Si HEMT (Al =0.22)	Random Telegraph Signal	Surface or buffer
Soh [5]	0.17/0.18	8.7×10^{-18} / 7.9×10^{-18}	3.5×10^{14} / 5.5×10^{13}	MOCVD	Un-doped and Si-doped GaN	DLTS	Defect clusters along screw and mixed dislocations
Faqir [12]	0.18	4.5×10^{-19}	-	MOCVD	GaN/AlGaN/GaN/ SiC HEMT (Si doped AlGaN)	DLTS	Surface trap
Martin [13]	0.18	-	-	MOCVD	InAlN/GaN/SiC HEMT (In =0.17)	DCT	Surface state defects
Sghaier [8]	0.19	4.2×10^{-15}	-	MOCVD	AlGaN/GaN/Si HEMT (Al =0.22)	Low Frequency dispersion	-

Cho [14]	0.19/0.23	2.43×10^{-16}/ 5.43×10^{-15}	5.0×10^{13} / 9.5×10^{13}	MOCVD	Un-doped GaN flims on Sapphire	DLTS	Edge dislocations
Gassoumi [3]	0.20	3.03×10^{-17}	-	MBE	AlGaN/GaN/Si HEMT	Conductance DLTS	GaN buffer or at the strained Si/AlN nucleation
Zhang [9]	0.2	2.1×10^{-14}	5.7×10^{14}	Ammonia MBE	n-type GaN (m-plane)	DLTS	-
Polyakov [15]	0.20	-	-	MOCVD	Un-doped c-plane GaN flims on r-plane Sapphire substrate	Photo Induced Current Transient Spectroscopy (PICTS)	N-vacancy
Fang [1]	0.20 – 0.21	8.4×10^{-17}, 1.6×10^{-14}	-	RMBE	Si doped n-GaN	DLTS	N-vacancy
Martin [13]	0.21	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.29)	DCT	Either AlGaN barrier or GaN buffer
Chikhaoui [6]	0.21	1.1×10^{-18}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.24)	Fourier Transform DLTS	Buffer/Interface states
Polyakov [16]	0.21	1×10^{-21}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.3)	Admittance spectroscopy	AlGaN barrier
Umano-Membreno [17]	0.21	3.6×10^{-17}	3.1×10^{13}	MOCVD	n-GaN flims (lightly Si doped GaN/Fe-doped GaN buffer	DLTS	Also found in HVPE and RMBE GaN layers
Jin [18]	0.23	-	-	MOCVD	AlGaN/GaN/SiC HEMT	Dynamic R_{ON}	AlGaN barrier

Olena [19]	0.23	-	-	MBE	GaN sample	Cathodoluminescence (CL) measurements	Fe-doped GaN
Arehart [20]	0.24	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLTS	N-vacancy
Soh [5]	0.24	2.6×10^{-18} / 4.5×10^{-18}	5.5×10^{14} / 8.8×10^{13}	MOCVD	Un-doped and Si-doped GaN	DLTS	Defect clusters along screw and mixed dislocations
Arehart [21]	0.24/0.25	-	6.0×10^{12} / 2.3×10^{14}	PA-MBE	n-type GaN grown on (N-face/ Ga-face)	DLTS	N-vacancy
Arehart [21]	0.25	-	3.5×10^{13}	PA-MBE	n-type GaN grown on Ga-face	DLTS	N-vacancy
Polyakov [15]	0.25	-	5.0×10^{13}	MOCVD	Un-doped c-plane GaN flims on r-plane Sapphire substrate	DLTS	Also observed in n-type GaN grown on C-plane by MOCVD
Young [11]	0.25	1.1×10^{-17}	9.4×10^{15}	Plasma-assisted MBE	GaN/AlGaN/ Sapphire HEMT (Al =0.2)	DLTS	Extended defects such as dislocations
Chen [7]	0.26	1.4×10^{-14}	-	HVPE	n-GaN flims	DLTS	Native defects (N or Ga-vacancy)
Umano-Membreno [4]	0.265	2.5×10^{-15}	4.3×10^{13}	MOCVD	Schottky diode on un-doped n-GaN)	Transient Capacitance Measurements	-
Gassoumi [22]	0.29	4.1×10^{-17}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.22)	Capacitance and Conductance DLTS	Region below the 2DEG channel

Jin [18]	0.31	-	-	MOCVD	AlGaN/GaN/SiC HEMT	Dynamic R_{ON}	AlGaN barrier
Gassoumi [22]	0.31	5.89×10^{-17}	-	MOCVD	AlGaN/GaN/SiC HEMT	Conductance DLTS	AlGaN layer
Sghaier [8]	0.31	1×10^{-16}	-	MOCVD	AlGaN/GaN/Si HEMT (Al =0.22)	Capacitance DLTS	AlGaN layer
Sghaier [8]	0.33	8.71×10^{-19}	-	MOCVD	AlGaN/GaN/ Al_2O_3 HEMT (Al =0.22)	Random Telegraph Signal	Surface or bulk
Heitz [23]	0.34	-	-	HVPE	GaN samples	Photoluminescence excitation (PLE)	Fe-doped GaN
Osaka [24]	0.348	2.64×10^{-15}	-	HVPE	n-AlGaN flims on sapphire (Al =0.09)	Capacitance DLTS	Point defect in AlGaN
Polyakov [16]	0.35	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.3) (Neutrons irradiated)	Admittance spectroscopy	AlGaN barrier
Umano-Membreno [30]	0.355	6.5×10^{-16}	1.7×10^{13}	MOCVD	Schottky diode on un-doped n-GaN (gamma irradiated)	Transient Capacitance Measurements	N-vacancy
Olena [19]	0.36	-	-	MBE	AlGaN/GaN sample (Al =0.2)	Cathodoluminescence (CL) measurements	Fe-doped AlGaN
Chikhaoui [25]	0.365	1.4×10^{-19}	-	MOCVD	AlInN/GaN/SiC HEMT (Al=0.72)	Fourier transform Current DLTS	AlInN/Metal interface
Chini [26]	0.37 – 0.42	-	-	MOCVD	AlGaN/GaN/SiC HEMTs (Fe-doped)	Drain current turn-on transient measurement	GaN buffer

Martin [13]	0.38	-	-	MOCVD	InAlN/GaN/SiC HEMT (In =0.17)	DCT	Structural defect in the InAlN barrier
Arehart [20]	0.40	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLTS	Common point defect
Soh [5]	0.40	5.2×10^{-17}	6.9×10^{13}	MOCVD	Si-doped GaN	DLTS	Si-doped induced defects
Chikhaoui [6]	0.42, 0.49	1.3×10^{-19}, 2.4×10^{-19}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.24)	Fourier Transform DLTS	Interface states
Martin [13]	0.43	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.29)	DCT	C/O/H impurities
Arehart [21]	0.44	-	5.0×10^{13}	PA-MBE	n-type GaN grown on N-face	DLTS	Origin unclear; Also found in N-face, n-GaN sample in ammonia MBE
Jin [18]	0.45	-	-	MOCVD	AlGaN/GaN/SiC HEMT	Dynamic R_{ON}	AlGaN barrier
Tapajna [27]	0.45	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.26)	Raman thermography and Electroluminescence (EL)	C/O related impurities defects
Polyakov [16]	0.45	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.3) (Neutrons irradiated)	Admittance spectroscopy	AlGaN barrier
Sasikumar [28]	0.45	-	4.1×10^{12} / 4.5×10^{12}	MBE	AlGaN/GaN HEMT (Al =0.28) Before/after stress	Constant drain current DLTS	Origin unclear

Osaka [24]	0.466	3.69×10^{-15}	-	HVPE	n-AlGaN flims on sapphire (Al =0.17)	Capacitance DLTS	Point defect in AlGaN
Jie Yang [29]	0.5	-	-	MBE	AlGaN/GaN HEMT	Electron Tunneling Spectroscopy	Bulk of AlGaN and AlGaN/GaN interface
Faqir [12]	0.5	5.0×10^{-16}	-	MOCVD	GaN/AlGaN/GaN/ SiC HEMT (Si doped AlGaN)	DLTS	Bulk trap
Cho [30]	0.5	4.65×10^{-17}, 4.96×10^{-17}	2.3×10^{14}, 1×10^{14}	MOCVD	n-type GaN (un-doped, In-doped)	DLTS	Nitrogen antisite point defect
Gassoumi [3]	0.5	2.57×10^{-15}	-	MBE	AlGaN/GaN/Si HEMT (Al =0.22)	Conductance DLTS	GaN buffer or at the strained Si/AlN nucleation
Kindl [31]	0.52	8.0×10^{-15}	1.5×10^{14}	LP-MVPE	GaN/AlGaN/SiC HEMT (Al =0.08)	DLTS	N_{Ga} antisite defect in AlGaN layer
Jin [18]	0.53, 0.57	-	-	MOCVD	AlGaN/GaN/SiC HEMT	Dynamic R_{ON}	AlGaN barrier
Umano-Membreno [17]	0.535	2.0×10^{-16}	2.7×10^{14}	MOCVD	n-GaN flims (lightly Si doped GaN/Fe-doped GaN buffer	DLTS	Nitrogen antisite defect
Axelsson [32]	0.54 – 0.63	-	-	MOCVD	AlGaN/GaN HEMTs (Fe-doped GaN Buffer)	Drain current Transient Measurements (DCTS)	Traps located in the GaN, whose properties are influenced by Fe-doping

Sghaier [8]	0.54	4.29×10^{-15}	-	MOCVD	AlGaN/GaN/Si HEMT (Al =0.22)	Random Telegraph Signal	Surface or Buffer
Sasikumar [28]	0. 54	-	5.4×10^{12}	MBE	AlGaN/GaN HEMT (Al =0.28) Before/after stress	Constant drain current DLTS	Also found in PA-MBE grown HEMTs
Stuchlikova [33]	0.545	2.8×10^{-16}	-	LP-MOVPE	AlGaN/GaN HEMT (Al =0.19)	DLTFS	Nitrogen antisite point defect (N_{Ga})
Cho [14]	0.55/0.60	2.8×10^{-16}/ 1.61×10^{-15}	1.4×10^{14} / 3.2×10^{14}	MOCVD	Un-doped GaN flims on Sapphire	DLTS	Could be N-antisite and N-interstitial
Bisi [34]	0.56	5.0×10^{-15}	-	MOCVD	AlGaN/GaN HEMT (Al =0.25) Fe-doped GaN buffer	DCTS	GaN buffer
Sasikumar [35]	0.57	3.0×10^{-13}	$\sim 7 \times 10^{12}$ – 8×10^{12}	MOCVD	InAlN/GaN and AlGaN/GaN on SiC HEMT	Constant drain current DLTS	GaN buffer
Cardwell [36]	0.57	1.5×10^{-15}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al=0.3) Fe-doped GaN buffer	Temperature dependent resistance transients (RTS)	Traps located in the GaN, whose concentration is influenced by Fe-doping
Arehart [33]	0.57	-	5.8×10^{12} / 7.6×10^{12}	MOCVD	AlGaN/GaN/SiC HEMT (Unstressed/Stressed)	Constant drain current DLTS	AlGaN surface
A. Chini [37]	0.57/ 0.58/ 0.59	5.86×10^{-15} / 5.13×10^{-15} / 2.24×10^{-14}	-	MOCVD	AlGaN/GaN HEMTs	Drain Current Transient Measurements	Fe-doped GaN buffer

Umano-Membreno [4]	0.581	1.4×10^{-15}	6.1×10^{13}	MOCVD	Schottky diode on un-doped n-GaN	Transient Capacitance Measurements	-
Asghar [38]	0.59	0.3×10^{-17}	2.2×10^{14}	MOCVD	GaN p-n diode	DLTFS	Native defects in GaN
Chen [39]	0.59	-	-	MOVPE	GaN n^{+} -p junction	DLTS	V_N-Mg complex defect
Soh [5]	0.59/0.62	9.0×10^{-16} / 5.0×10^{-16}	8.5×10^{13} / 9.0×10^{13}	MOCVD	Un-doped and Si-doped GaN	DLTS	Linear array of defects due to dangling bonds along edge dislocations
Stuchlikova [33]	0.599	2.9×10^{-17}	-	LP-MOVPE	AlGaN/GaN HEMT (Al =0.19)	DLTFS	Ga-vacancy and O_N
Cho [30]	0.6	1.61×10^{-15}, 1.29×10^{-15}	3.2×10^{14}, 3.5×10^{14}	MOCVD	n-type GaN (un-doped, Si-doped)	DLTS	Nitrogen antisite point defect
Polyakov [15]	0.6	-	2.5×10^{14}	MOCVD	Un-doped c-plane GaN flims on r-plane Sapphire substrate	DLTS	Also observed in n-type GaN grown on C-plane by MOCVD
Arehart [21]	0.6	-	1.9×10^{13}	PA-MBE	n-type GaN grown on Ga-face	DLTS	Complex point defect
Chung [10]	0.601	5.80×10^{-15}, 3.97×10^{-15}	8.49×10^{14}, 1.43×10^{14}	MOVPE	GaN flim (un-doped and In-doped)	DLTS	Native defects or N antisite point defect
Chen [7]	0.61	6.8×10^{-15}	-	HVPE	n-GaN flims	DLTS	Native defects (N_{Ga} related)

Bisi [40]	0.62	8.7×10^{-15}	-	MOCVD	AlGaN/GaN/SiC HEMT	DCT	GaN point defect
Arehart [20]	0.62	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLTS	Origin unclear
Hierro [41]	0.62	6×10^{-15}	-	MOCVD	n-GaN flim	DLTS	Mg-H complex in n-GaN
Gassoumi [42]	0.63	5.9×10^{-14}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al = 0.25)	Conductance DLTS	Nitrogen antisite point defect
Matteo [43]	0.63	-	-	MOCVD	AlGaN/GaN/SiC HEMT (Fe-doped GaN buffer)	Drain current Transient (DCT)	GaN buffer, whose properties depends on the concentration of Fe-doping
Matteo [44]	0.63	2.3×10^{-14}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.25)	DCT	Located in the GaN buffer. Intrinsic defects or impurities such as carbon
Stuchlikova [33]	0.642	1.8×10^{-17}	-	LP-MOVPE	AlGaN/GaN HEMT (Al =0.19)	DLTFS	Ga-vacancy and O_N
Arehart [21]	0.65/0.66	-	3.6×10^{13} / 1.4×10^{13}	PA-MBE	n-type GaN grown on (N-face/Ga-face)	DLTS	Nitrogen related defects
Chen [7]	0.65 – 0. 70	$\sim 5 \times 10^{-17}$	-	HVPE	n-GaN flims	DLTS	Electron beam irradiated induced defect

Kindl [31]	0.66	1.0×10^{-14}	2.0×10^{14}	LP-MVPE	GaN/AlGaN/SiC HEMT (Al =0.08 and 0.3)	DLTS	N Interstitials in the AlGaN nucleation layer
Zhang [9]	0.66	8.9×10^{-13}/ 1.1×10^{-15}	4.2×10^{14}	Ammonia MBE	n-type GaN (m/c-plane)	DLTS	-
Silvestri [45]	0.66/0.68/0.7	$(1/4/8)\times10^{-13}$	-	MOVPE	AlGaN/GaN/SiC HEMTs (Al =0.22) (Medium/ High/Low Fe-doped GaN buffer)	Transconductance frequency dispersion	Traps located in GaN buffer, whose energy levels and cross sections are influenced by Fe-doping.
Osaka [24]	0.691	9.76×10^{-16}	-	HVPE	n-AlGaN flims on sapphire (Al =0.09)	Capacitance DLTS	Point defect in AlGaN
Silvestri [46]	0.7	8×10^{-13}	-	MOVPE	AlGaN/GaN/SiC HEMT (Fe doped GaN)	Transconductance frequency dispersion	GaN bulk
Arehart [20]	0.72	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLTS	Common point defect
Jin [18]	0.75	-	-	MOCVD	AlGaN/GaN/SiC HEMT	Dynamic R_{ON}	AlGaN barrier
Asghar [38]	0.76	1.5×10^{-17}	5.33×10^{14}	MOCVD	GaN p-n diode	DLTFS	Nitrogen Interstitials
Faqir [12]	0.76	2.0×10^{-15}	-	MOCVD	GaN/AlGaN/GaN/ SiC HEMT (Si doped AlGaN)	DLTS	Bulk trap

Umano-Membreno [17]	0.795 – 0.800	2.1×10^{-17} - 2.3×10^{-17}	0.1×10^{14} – 1.4×10^{13}	MOCVD	n-GaN flims (lightly Si doped GaN/Un-doped GaN/Fe-doped and Un-doped GaN buffer/Sapphire	DLTS	Also found in HVPE and RMBE GaN layers
Kindl [31]	0.80	5.0×10^{-14}	8.0×10^{14}	LP-MVPE	GaN/AlGaN/SiC HEMT (Al =0.08 and 0.3)	DLTS	Point defect in AlGaN nucleation layer
Osaka [24]	0.808	1.40×10^{-15}	-	HVPE	n-AlGaN flims on sapphire (Al =0.09)	Capacitance DLTS	Point defect in AlGaN
Martin [13]	0.82	-	-	MOCVD	InAlN/GaN/SiC HEMT (In =0.17)	DCT	Material growth
Gassoumi [3]	0.83	3.14×10^{-17}	-	MBE	AlGaN/GaN/Si HEMT	Conductance DLTS	GaN buffer or at the strained Si/AlN nucleation
Kindl [31]	0.83	5.0×10^{-16}	3.0×10^{14}, $< 1 \times 10^{13}$	LP-MVPE	GaN/AlGaN/SiC HEMT (Al =0.08 and 0.3)	DLTS	Origin unclear
Kamyczek [47]	0.83	2×10^{-13}	7.4×10^{16}	MOVPE	p-i-n GaN junction	Laplace DLTS	Could be intrinsic defect
Fang [1]	0.85	-	-	MOCVD	n-type GaN (electron irradiated)	DLTS	Nitrogen Interstitials
Jin [18]	0.87	-	-	MOCVD	AlGaN/GaN/SiC HEMT	Dynamic R_{ON}	AlGaN barrier
Arehart [48]	0.87/0.9	9.0×10^{-13}	-	MOCVD	AlGaN/GaN Schottky diode (Al =0.3)	DLTS/DLOS	Origin unclear

Osaka [24]	0.898	8.09×10^{-15}	-	HVPE	n-AlGaN flims on sapphire (Al =0.17)	Capacitance DLTS	Point defect in AlGaN
Bisi [40]	0.91	3.3×10^{-13}	-	MOCVD	AlGaN/GaN/SiC HEMT	DCT	Gallium vacancy point defect
Chikhaoui [6]	0.94	1.1×10^{-22}	-	MOCVD	AlGaN/GaN/SiC HEMT (Al =0.24)	Fourier Transform DLTS	Line defects
Asghar [38]	0.96	7.67×10^{-16}	1.71×10^{15}	MOCVD	GaN p-n diode	DLTFS	Nitrogen Interstitials associated with Ga-vacancy or a complex defect
Kamyczek [47]	0.99	5.0×10^{-12}	1.5×10^{16}	MOVPE	AlGaN/GaN heterojunction	Laplace DLTS	Could be intrinsic defect
Fang [49]	1.0	2.0×10^{-12}	-	MOCVD	AlGaN/GaN/SiC Schottky barrier diode (with and without passivation)	DLTS	Threading dislocations
Arehart [50]	1.0	-	1.4×10^{12}	MOCVD	AlGaN/GaN/SiC HEMT (Stressed)	Constant drain current DLTS	GaN or AlGaN layer
Bisi [40]	1.1	3.9×10^{-12}	-	MOCVD	AlGaN/GaN/SiC HEMT	DCT	GaN dislocations
Stuchlikova [33]	1.118	1.4×10^{-13}	-	LP-MOVPE	AlGaN/GaN HEMT (Al =0.19)	DLTFS	Ga-vacancy and O_N
Arehart [20]	1.28	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLOS	Carbon impurities
Arehart [50]	1.3	-	$\sim 5 \times 10^{11}$	MOCVD	AlGaN/GaN/SiC HEMT (Stressed)	Constant drain current DLOS	GaN or AlGaN layer

Arehart [48]	1.5	-	-	MOCVD	AlGaN/GaN Schottky diode (Al =0.3)	DLOS	Origin unclear
Sghaier [8]	1.8	3.0×10^{-16}	-	MOCVD	AlGaN/GaN/Si HEMT (Al =0.22)	Frequency dispersion	-
Klein [51], [52]	1.8	-	-	OMCVD and MBE	AlGaN/GaN HEMT	Photoionization spectroscopy	Located in GaN buffer
Arehart [50]	1.9	-	$\sim 2\times 10^{12}$	MOCVD	AlGaN/GaN/SiC HEMT (Stressed)	Constant drain current DLOS	GaN or AlGaN layer
Sasikumar [28]	2.3	-	4.7×10^{11} / 5.7×10^{11}	MBE	AlGaN/GaN HEMT (Al =0.28) Before/after stress	Constant drain current DLOS	Also found in PA-MBE grown HEMTs
Zhang [9]	2.47/2.49	-	-	Ammonia MBE	n-type GaN (m-plane)	DLTS	V_{Ga} and V_{Ga}-H states
Arehart [20]	2.62	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLTS	N-vacancy
Arehart [21]	2.62	-	9.0×10^{13} / 8.5×10^{13}	PA-MBE	n-type GaN grown on (N-face/Ga-face)	DLTS	Ga-vacancy
Klein [51], [52]	2.85	-	-	OMCVD and MBE	AlGaN/GaN HEMT	Photoionization spectroscopy	Gallium vacancy
Arehart [48]	3.11	-	-	MOCVD	AlGaN/GaN Schottky diode (Al =0.3)	DLOS	Native Cation vacancy
Zhang [9]	3.24/3.26	-	-	Ammonia MBE	n-type GaN (c-plane)	DLTS	C_N substitutional impurities
Arehart [20]	3.28	-	-	Ammonia MBE	n-type GaN Schottky diodes	DLTS	CN substitutional

Sasikumar [28]	3.28	-	3.4×10^{11}	MBE	AlGaN/GaN HEMT (Al =0.28) Before/after stress	Constant drain current DLOS	Carbon defect in GaN
Arehart [50]	3.76	-	$\sim 7.0 \times 10^{11}$	MOCVD	AlGaN/GaN/SiC HEMT (Stressed)	Constant drain current DLOS	AlGaN layer
Arehart [48]	3.93	-	-	MOCVD	AlGaN/GaN Schottky diode (Al =0.3)	DLOS	Mg impurities

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Physics-Based TCAD Device Simulations and Measurements of GaN HEMT Technology for RF Power Amplifier Applications

Abstract: GaN High Electron Mobility Transistors (HEMTs) have demonstrated their capabilities to be an excellent candidate for high power microwave and mm-wave applications. However, the presence of traps in the device structure significantly degrades the device performance and also detriments the device reliability. Moreover, the origin of these traps and their physical location remains unclear till today. A part of the research work carried out in this thesis is focused on characterizing the traps existing in the GaN/AlGaN/GaN HEMT devices using LF S-parameter measurements, LF noise measurements and drain-lag characterization. Furthermore, we have used TCAD-based physical device simulations in order to identify the physically confirm the location of traps in the device. Moreover, our experimental characterization and simulation study suggest that LF measurements could be an effective tool for characterizing the traps existing in the GaN buffer whereas gate-lag characterization could be more useful to characterize the AlGaN barrier traps of GaN HEMT devices.

The second aspect of this research work is focused on characterizing the AlN/GaN/AlGaN HEMT devices grown on Si and SiC substrate. We attempt to characterize the temperature-dependent on-resistance (R_{ON}) extraction of these devices using on-wafer measurements and TCAD-based physical simulations. Furthermore, we have proposed a simplified methodology to extract the temperature and bias-dependent channel sheet resistance (R_{sh}) and parasitic series contact resistance (R_{se}) of AlN/GaN HEMT devices. Further, we have made a comprehensive evaluation of thermal behavior of these devices using on-wafer measurements and TCAD-based three-dimensional (3D) thermal simulations. The thermal resistance (R_{TH}) has been extracted for various geometries of the device using measurements and validated using TCAD-thermal simulations.

Keywords: GaN HEMT, Trapping effects, LF S-parameter measurements, Noise measurements, TCAD physical simulations, Analytical modeling, Thermal modeling.

Simulations physiques et mesures du composant de technologie GaN HEMT pour les applications d'amplificateur de puissance RF

Résumé: Depuis plusieurs années, la technologie de transistors à effet de champ à haute mobilité (HEMT) sur Nitrure de Gallium (GaN) a démontré un potentiel très important pour la montée en puissance et en fréquence des dispositifs. Malheureusement, la présence des effets parasites dégrade les performances dynamiques des composants ainsi que leur fiabilité à long-terme. En outre, l'origine de ces pièges et leur emplacement physique restent incertains jusqu'à aujourd'hui. Une partie du travail de recherche menée dans cette thèse est axée sur la caractérisation des pièges existant dans les dispositifs HEMTs GaN à partir de mesures de paramètre S basse fréquence (BF), les mesures du bruit BF et les mesures I(V) impulsionnelles. Parallèlement, nous avons effectué des simulations physiques basées sur TCAD afin d'identifier la localisation des pièges dans le transistor. De plus, notre étude expérimentale de caractérisation et de simulation montre que les mesures BF pourraient constituer un outil efficace pour caractériser les pièges existant dans le buffer GaN, alors que la caractérisation de Gate-lag pourrait être plus utile pour identifier les pièges de barrièredes dispositifs GaN HEMT..
La deuxième partie de ce travail de recherche est axée sur la caractérisation des dispositifs AlN/GaN HEMT sur substrat Si et SiC. Une méthode d'extraction simple et efficace de la résistance canal et de la résistance de contact a été mise au point en utilisant conjointement la simulation physique et les techniques de caractérisation. Le principe de l'extraction de la résistance canal est basée sur la mesure de la résistance R_{ON}. Celle-ci est calculée à partir des mesures de courant de drain I_{DS} et de la tension V_{DS} pour différentes valeurs de températures En outre, nous avons procédé à une évaluation complète du comportement thermique de ces composants en utilisant conjointement les mesures et les simulations thermiques tridimensionnelles (3D) sur TCAD. La résistance thermique (R_{TH}) a été extraite pour les transistors de différentes géométries à l'aide des mesures et ensuite validée par les simulations thermiques sur TCAD.

Mots clés: HEMT GaN, Pièges, mesure de paramètres-[S] BF, mesures de bruit BF, simulations physiques sur TCAD, modélisation analytique, modélisation thermique.