

Université de Limoges

ED 610 – Sciences et Ingénierie des Systèmes, Mathématiques, Informatique (SISMI)
Faculté des Sciences et Techniques – Institut de Recherche XLIM

Thèse pour obtenir le grade de
Docteur de l'Université de Limoges
Électronique des Hautes Fréquences, Photonique et Systèmes

Présentée et soutenue par

Rémy BOUCHÉ

Le 21 Décembre 2021

CONCEPTION HYBRIDE DE FONCTIONS HYPERFRÉQUENCES ET NUMÉRIQUES EN TECHNOLOGIE SiGe POUR ANTENNE À BALAYAGE ÉLECTRONIQUE EN BANDE KA DESTINÉE AUX TÉLÉCOMMUNICATIONS SATELLITAIRES

Thèse dirigée par Bernard JARRY et Julien LINTIGNAT

JURY :

Président du jury

M. Stéphane BILA, Directeur de Recherche CNRS – XLIM – Université de Limoges

Rapporteurs

M. Philippe FERRARI, Professeur – RFIC Lab – Université Grenoble Alpes

M. Eric RIUS, Professeur – Lab-STICC – Université de Brest

Examineurs

M. Bruno BARELAUD, Professeur – XLIM – Université de Limoges

M. Bernard JARRY, Professeur – XLIM – Université de Limoges

M. Julien LINTIGNAT, Maître de Conférences – XLIM – Université de Limoges

M. Philippe MEUNIER, Ingénieur – NXP Semiconductors – Caen

Invités

M. Benoît LESUR, Ingénieur – Safran Data Systems – La Teste-de-Buch



Dédicace [à compléter]

Vous pouvez inscrire ici une citation, par exemple :

If I have seen further, it is by standing on the shoulders of Giants.

Sir Isaac Newton

Remerciements

Écrivez vos remerciements dans cette rubrique (professeurs, amis, famille, etc).

Droits d'auteurs

Cette création est mise à disposition selon le Contrat :

« Attribution-Pas d'Utilisation Commerciale-Pas de modification 3.0 France »

disponible en ligne : <http://creativecommons.org/licenses/by-nc-nd/3.0/fr/>



Table des Matières

1	Introduction	9
1.1	Disclaimer	10
1.2	Examples	11
2	Layout techniques for mm-Wave design in silicon	13
2.1	Layout Design Methodology	14
2.2	Investigations on mm-Wave co-design	18
2.2.1	Reference plane influence over design	21
2.3	mm-Wave design simulation	22
2.4	Discussion	24
A	Annexes	25
A.1	Free-space path loss	26
A.2	Noise calculation in 2-port systems	29
B	Bibliographie	32
	Références	33
	Liste des travaux	34

Table des Figures

1.1	Bandes ISM 60 GHz	11
2.1	Design flow for analog circuit design emphasizing layout design steps. .	16
2.2	Examples of different methods of circuit extraction from layout.	17
2.3	Circuit simulated with different extraction methods.	17
2.4	Comparison of simulation on input impedance of same circuit and with different extraction types.	18
2.5	Comparison of measured 60 GHz LNA and simulation results in different modes of extraction.	20
2.6	Passive section of the second version of filtering LNA design.	21
2.7	Reference plan influence over resonator circuit design.	22
2.8	Proposed concurrent design flow for analog circuit.	23
2.9	Test-bench example for multiple extraction design used in this work. . .	23

Liste des Abréviations

- 4G** – Fourth Generation Mobile Radio.
- CAD** – Computer-Aided Design.
- DRC** – Design Rule Check.
- EM** – Electromagnetic.
- GSG** – Ground-Signal-Ground.
- ISM** – Industrial, Scientific and Medical.
- LNA** – Low-Noise Amplifier.
- LVS** – Layout Versus Schematic.
- mm-wave** – Millimeter-Wave.
- PDK** – Process Design Kit.
- RF** – Radio Frequency.
- RFIC** – Radio-Frequency Integrated Circuits.

1

Introduction

Sommaire

1.1	Disclaimer	10
1.2	Examples	11

1.1 Disclaimer

Ce modèle Latex pour les thèses de doctorat à l'Université de Limoges par Benoît Crespin (benoit.crespin@unilim.fr), sur la base de documents rédigés au fil des années par différents doctorants à l'institut XLIM, notamment Rémy Bouché.

Le modèle se conforme aux recommandations du SCD de l'université (Service Commun de la Documentation) :

<https://support.unilim.fr/publications-et-redaction/depot-et-modeles-de-documents/telecharger-un-modele-de-document/>

La plateforme en ligne Overleaf (<https://fr.overleaf.com>) a été utilisée pour le développement, néanmoins n'importe quel éditeur \LaTeX devrait fonctionner pour éditer les fichiers. Pour utiliser ce modèle vous devez avoir une connaissance minimale du langage \LaTeX de façon à pouvoir personnaliser certains éléments, qui se trouvent dans différents fichiers :

- `thesis.tex` est le document principal qui contient notamment le titre de la thèse, la date, l'école doctorale, etc.
- le dossier `source` contient plusieurs fichiers correspondant à la page de garde, la dédicace, les remerciements, etc.
- `unilim.cls` est le fichier de style définissant la plupart des paramètres, a priori vous n'avez pas besoin de le modifier

Quelles que soient les modifications apportées vous pouvez vous référer à la page du SCD pour comparer avec les modèles Word fournis, notamment de façon à respecter le format de la page de garde et de la dernière page (comportant un résumé en français et en anglais).

Dernière version : 6 janvier 2022

1.2 Examples

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetur id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum. , [1], [2] and [3]:

1. Data rates of tens of megabits per second for tens of thousands of users;
2. Data rates of 100 megabits per second for metropolitan areas;
3. 1 Gbps simultaneously to many workers on the same office floor;
4. Several hundreds of thousands of simultaneous connections for wireless sensors;
5. Spectral efficiency significantly enhanced compared to Fourth Generation Mobile Radio (4G);
6. Coverage improved;
7. Signaling efficiency enhanced.

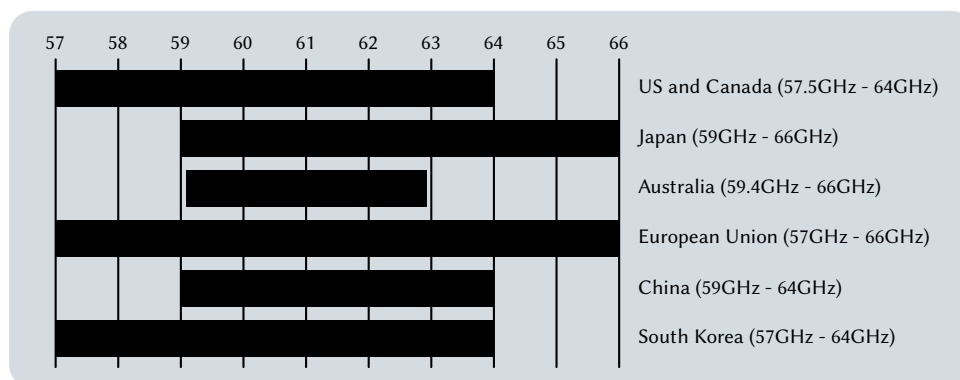


Figure 1.1: Bandes ISM 60 GHz

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Ut purus elit, vestibulum ut, placerat ac, adipiscing vitae, felis. Curabitur dictum gravida mauris. Nam arcu libero, nonummy eget, consectetur id, vulputate a, magna. Donec vehicula augue eu neque. Pellentesque habitant morbi tristique senectus et netus et malesuada fames ac turpis egestas. Mauris ut leo. Cras viverra metus rhoncus sem. Nulla et lectus vestibulum urna fringilla ultrices. Phasellus eu tellus sit amet tortor gravida placerat. Integer

sapien est, iaculis in, pretium quis, viverra ac, nunc. Praesent eget sem vel leo ultrices bibendum. Aenean faucibus. Morbi dolor nulla, malesuada eu, pulvinar at, mollis ac, nulla. Curabitur auctor semper nulla. Donec varius orci eget risus. Duis nibh mi, congue eu, accumsan eleifend, sagittis quis, diam. Duis eget orci sit amet orci dignissim rutrum. Nam dui ligula, fringilla a, euismod sodales, sollicitudin vel, wisi. Morbi auctor lorem non justo. Nam lacus libero, pretium at, lobortis vitae, ultricies et, tellus. Donec aliquet, tortor sed accumsan bibendum, erat ligula aliquet magna, vitae ornare odio metus a mi. Morbi ac orci et nisl hendrerit mollis. Suspendisse ut massa. Cras nec ante. Pellentesque a nulla. Cum sociis natoque penatibus et magnis dis parturient montes, nascetur ridiculus mus. Aliquam tincidunt urna. Nulla ullamcorper vestibulum turpis. Pellentesque cursus luctus mauris.

2

Layout techniques for mm-Wave design in silicon

Sommaire

2.1	Layout Design Methodology	14
2.2	Investigations on mm-Wave co-design	18
2.2.1	Reference plane influence over design	21
2.3	mm-Wave design simulation	22
2.4	Discussion	24

SIMULATION-driven circuit design becomes more and more important in microelectronic industry due to the necessity of fast execution for production. Although the design work-flow changes for different circuits specifications, it is based on a well known and secure design procedure that guarantee error-prone devices. However, new technologies keep tightening design constraints in frequency, consumption size and others, and it turns out that the use of a classical design approach has to be constantly reevaluated due to different problems introduced with the miniaturization of the technology. In this chapter, an algorithmic method for Radio-Frequency Integrated Circuits (RFIC) design – validated with an LNA design – for mm-wave using Computer-Aided Design (CAD) tools (Cadence® Virtuoso® and ADS® Momentum®) is demonstrated. Information about how to perform with proposed work-flow and further discussion is also suggested in the last section.

2.1 Layout Design Methodology

Classically a Low-Noise Amplifier (LNA) design is done taking into consideration the requirements of the reception-chain for a given system transceiver (frequency, bandwidth, consumption, gain, noise, etc.), the objective is therefore to design a circuit that best fits its specifications. To perform this assignment a general design flow is roughly described in [4] and [5], although it is not a closed rule process design can be divided into three steps before production: circuit requirement identification (which includes schematic analysis and simulation), layout design, and initial fabrication for evaluation. By that, during circuit RFIC LNA design, a not extensive list of tasks the designer have to perform is:

1. System specification:
 - Mitigate specifications and determine which technology should be used, if the case.

- Determine which topology best fits to specifications.
- Choose transistor(s) to be used in design that meet required noise, if the case.
- Adapt the amplifier for noise and gain, in LNA design.
- Develop a preliminary design of circuit.
- Compute circuit design to evaluate if it meets specification

2. Layout design

- Sketch the circuit blueprint.
- Draw the layout design.
- Extract circuit from layout design.
- Compare layout and schematic responses, then determine if design meet specifications.

3. Evaluation tests

- Measure fabricated circuit and compare with simulation results.

For high-frequency Millimeter-Wave (mm-wave) design the designer have to care about the wavelength of the Radio Frequency (RF) signal. For mm-wave circuits, lumped element analysis can be inaccurate because the dimensions of the designed circuit can have the same order of magnitude of the signal wavelengths. Consequently, to ensure that the layout performs well the designer has to be familiar with distributed circuit elements and transmission-line theory.

More advanced designs need also that the designer be familiar with CAD software, considering that manual synthesis for complex mm-wave circuits become quickly impracticable primarily due to realization time. Nowadays, CAD software (notably Cadence® Virtuoso® and Keysight® ADS®) offers a great simulation environment to realize fabricated circuits that fit well with simulated results.

On the classical design flow approach, it is first set the conditions and requirements of the circuit (technology, topology, transistors, etc.). After, we proceed with the second stage, when the definition and validation of the schematic of the circuit is done. Only then the layout design stage begins, as illustrated in Figure 2.1.

Good layout design practice includes within its firsts steps discussions about the blueprint of the circuit layout. This blueprint has to contain the placement of each component (or each part) of the circuit and it have to be in accordance with the Design Rule Check (DRC) of the technology. The DRC is an operation which assures that the designed layout masks are in conformity with the rules of fabrication. After the circuit is completed the next move is to test the layout against its schematic version; thus the designer knows effectively if all circuit components are present in its layout version. This procedure is called Layout Versus Schematic (LVS) test.

After LVS is completed with no mistakes, the next step is to perform circuit extraction. Circuit extraction is the process of derivation of a schematic version of the layout, with

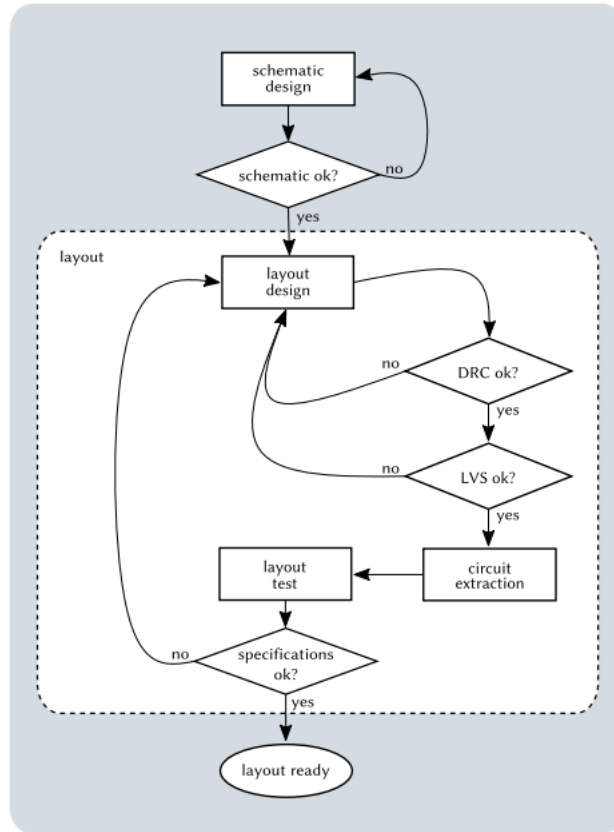


Figure 2.1: Design flow for analog circuit design emphasizing layout design steps.

its circuit interferers (intrinsic from layout) taken into account. This action is important because the designer can efficiently test the layout and determine if its response fit with the system design specification. In case the extracted version simulation results are not in accord with what is attended, then corrections must be performed in the layout.

Circuit extraction software can support different modes of layout circuit extraction. A general example is presented in Figure 2.2 where various methods of extractions are shown. In Figure 2.2 *R* stands for resistive extraction, *C* for capacitive extraction, *L* for inductive extraction and *K* for coupling interference between circuit metal connections, this last is represented with arrows in *RLCK* extraction.

Note that extraction examples in Figure 2.2 depend on the employed software and its context. For example, a designer wants to extract his layout and decided to use *R* extraction with $25\text{ }\mu\text{m}$ of circuit division. Assuming that the developed design is a piece of metal measuring $100 \times 10\text{ }\mu\text{m}^2$, then the parasite extractor can divide the circuit into four resistors with $R = 25 \times 10 \times R_{\square}\text{ }\Omega$. In other words, circuit extraction depends on the choice of designer and how the circuit will be divided by the extractor software.

Parameter setting for extraction is challenging because it is highly dependent on the circuit and its specifications. That means that setting bad extraction parameter values can

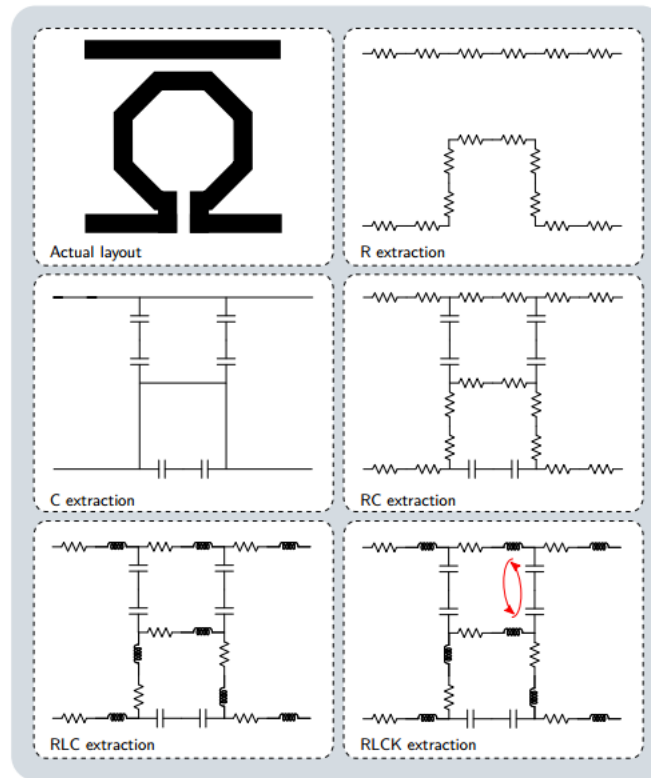


Figure 2.2: Examples of different methods of circuit extraction from layout.

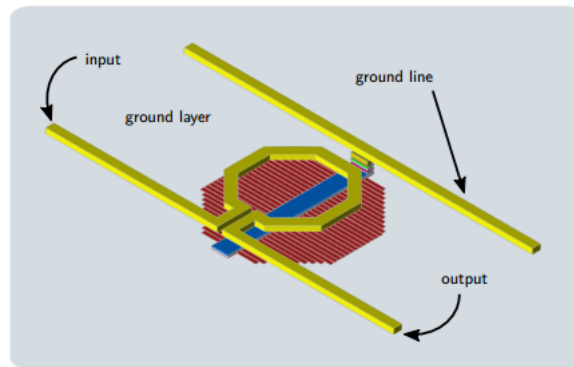


Figure 2.3: Circuit simulated with different extraction methods.

lead to completely different (and sometimes wrong) results. For example, the layout of Figure 2.3, was simulated to evaluate its S-parameter performance according to different types of circuit extractions. The tools used in this example were ASSURA[®] QRC for the circuit extractions and Keysight[®] Momentum[®] to Electromagnetic (EM) simulation, the schematic response was included in the graph of Figure 2.4 for comparative purposes. The layout in Figure 2.4 is composed of a one turn octagonal inductance with a line of $100 \times 10 \mu\text{m}^2$ on both the input and the output access, a ground line connect to

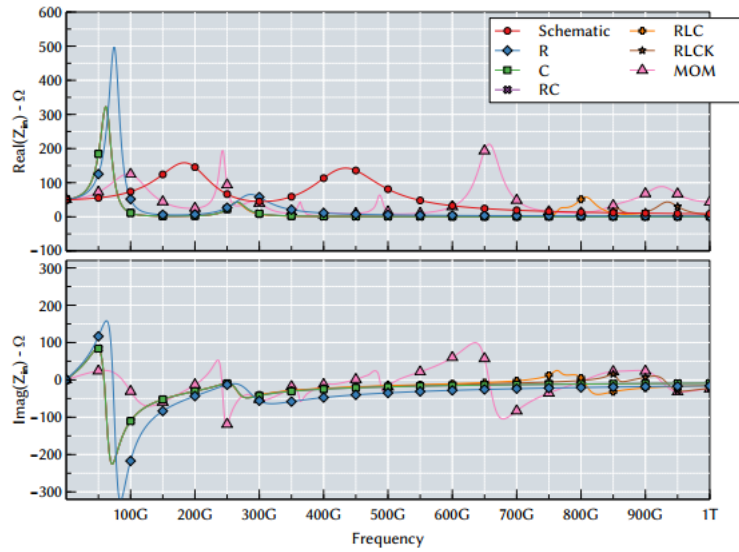


Figure 2.4: Comparison of simulation on input impedance of same circuit and with different extraction types.

the inductance ground layer. Figure 2.4 illustrates the input impedance results for the circuit with different kinds of extraction, including EM simulation. Inductance value and metal dimensions are not important in this example because we want to stress the difference within the curves response for the same circuit as motivation to investigate different extraction methods.

Simulations can lead to erroneous result interpretations due to its high dependency on the choice of extraction parameters, the fact that the technology component cells are modeled as a black-box, and therefore some parasites are not well modeled, also happens to be a problem because only the connected metal lines have the parasites computed. This way the simulation results rely on the modeled parasitics of each technology component.

Additionally, note that R, C, RC, RLC and RLCK extractions in the example give virtually the same frequency response (Figure 2.4), this result corroborates with the statement that the circuit is better modeled as a distributed-element circuit, because ASSURA® cannot model the interferers of the inductor. Furthermore, EM simulation gives a completely different result. At this point, the only information collected was that no extraction techniques were reliable because none comparison structure was available.

2.2 Investigations on mm-Wave co-design

Because in mm-wave wavelength (30 GHz to 300 GHz) varies between $1 \text{ cm} \leq \lambda \leq 1 \text{ mm}$ in free-space, and silicon design circuit dimensions have usually same order of mag-

nitude (normally hundreds of μm^2), phase change effects cannot be neglected. Also, the dimensions of the circuits designed in this work are bigger than the normal due to the co-design strategy. This means that the full circuit can be designed in a row, and therefore the circuit itself is electrically larger than the isolated circuit components.

Thus it is necessary to analyze different extraction modes to better adapt the design flow to the circuits being projected. Typically, EM modeling is preferred to problems of distributed elements, but different extraction modes have been evolving and worth to be investigated

During the investigation, five circuits were sent to fabrication within three fabrication runs. The circuit sent in the first run was a 60 GHz LNA working on Industrial, Scientific and Medical (ISM) band. After on the second run, two circuits were sent, an octagonal ring resonator filter, and a filtering 60 GHz LNA that uses the octagonal ring filter. Finally, in the last run, we sent a meander version of the filtering 60 GHz LNA and the meander filter itself. The meander ring filter is a smaller version of the ring resonator.

The first circuit (LNA 60 GHz) was realized within a workflow with only RLCK circuit extraction. No EM simulation was performed. This simulation choice was taken because circuit layout had $750 \times 520 \mu\text{m}^2$, therefore with width of about six times smaller than the signal wavelength at 60 GHz in freespace ($\lambda_{@60\text{ GHz}} \approx 5\text{ mm}$). Therefore simulated results were expected to be good approximations of circuit response.

Even though RLCK circuit extraction have performed well during s-parameters comparison with measurements (Figure 2.5, left side), frequencies nearby 60 GHz s-parameters begin to deviate. Parameter S_{11} , for example, shows a drop at 60 GHz that not meet simulations. Furthermore, although the measurements and simulation values are not exactly the same, it can be seen that EM modeling follow the same tendency.

In addition, in the right side of Figure 2.5 is shown the absolute error in log scale between different extraction modes and measurement ($E_a = |S_{\text{measure}} - S_{\text{simulation}}|$), so it is possible to analyze the extraction parameters more systematically, it is seen that although gain (S_{21}) is better represented using RLCK extraction (smaller error), Momentum® modeling error is more constant. For the other parameters (S_{11} and S_{22}) RLCK extraction shows higher error than on EM modeling, while small response drops happen with all extraction methods.

From the S-parameter error calculated due to simulation and measurements (Figure 2.5) we can speculate that, although the error is smaller on RLCK extractinon for frequencies bellow 60 GHz, in the parameter S_{21} , the error with EM extraction have less variation, further the error is even smaller on the other parameters (S_{11} and S_{22}).

The second active circuit set to fabrication was a version of the LNA connected with a filter, hence a filtering LNA that is intended to be a part of this work objective. During the design stage, the circuit was developed cascading the circuits (first stage amplifier, filter resonator, the second and third amplifier resonator connected in cascade). The

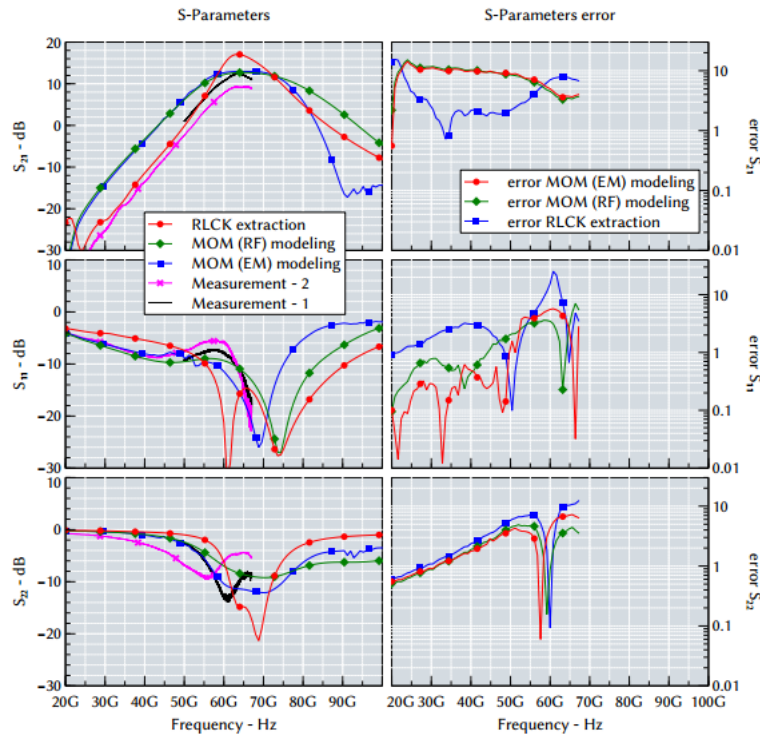


Figure 2.5: Comparison of measured 60 GHz LNA and simulation results in different modes of extraction. First column show s-parameters of measured and simulated structures, second column is the corresponding absolute error of simulations related to the measurement of each s-parameter.

resonator was electromagnetically simulated because RLCK circuit extraction does not model appropriately the resonant effect of the ring. Also, this simulation workflow was used because the circuit size was 1.34 mm^2 , and so it was expected unimportant phase delay along layout realization.

Standing that during simulations it was virtually granted that both structures (resonator and cascode stages) were optimally adapted, and it would be expected that the simulation response of the full circuit was correct. It happens that due to the circuit size and its characteristics, the reference plane is not electrically the same over the IC, what should be taken into account during the design. And therefore, the first version of filtering LNA did not perform as expected¹.

Hence, it is important to take advantage of CAD design in order to evaluate different configurations of the reference plane and better investigate the behavior of the circuit. For example, the second version of filtering LNA (Figure 2.6) was proposed with a more compact version of the resonator filter, and a different topology. Electromagnetic

¹Full circuit description is given in [insert ref]

modeling of the full passive part of the circuit was performed in order to describe and optimize its behavior.

EM circuit modeling is performed taking into account all interactions of the circuit parasites. Every connection between passive and/or active component on the circuit is modeled as a Momentum® port in the EM model and further connected to the active parts of the circuit. This way it is also possible to be aware of about the reference plane interactions with the circuit components.

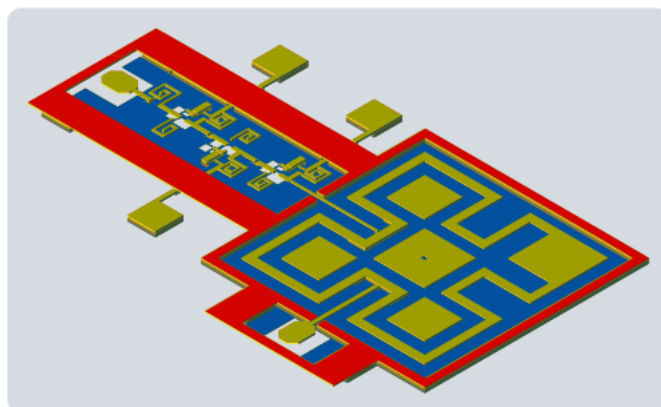


Figure 2.6: Passive section of the second version of filtering LNA design.

In the design of Figure 2.6 all the plane in red and blue is the ground plane (reference) connected with *vias* going from metal one up to metal six. Circuit ground pads are connected using Ground-Signal-Ground (GSG) probes, and therefore reference is not the same all over the circuit.

2.2.1 Reference plane influence over design

Reference plane carries out great importance on mm-wave circuit design. That happens because the wavelength of the irradiated signal is of the same order of magnitude of the circuit, as aforementioned. For example, Figure 2.7 illustrates the different responses of the filter resonator used in the second version of the filtering LNA due to different port configuration. Note that the response changes with different ground port positions.

In the upper design of Figure 2.7 red dots mark stacked differential ports configuration, in this configuration both signal and ground ports, are connected on metal six (*yellow*) and metal one (*blue*).

In the bottom design of Figure 2.7 red dot performs the same way that in the last design, blue and green dots are two parts of the differential port were blue dot is the signal port and green dot is ground port. It is seen that s-parameters differ from last design due to ground ports placement, what influences the filter circuit adaptation to

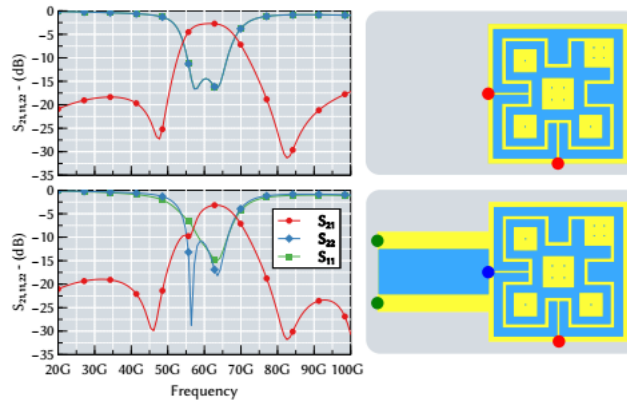


Figure 2.7: Reference plan influence over resonator circuit design.

the active part of the circuit, that in this case must be placed before the resonator, and connected to RF input of the filter (blue dot).

The difference in the simulation response implies that the designer has to perform the simulations according to the circuit connection during usage (measurements). The impact of these steps for co-design methodologies is that: first, the number of EM simulations can grow fast, and therefore the time spent on the design; second, the blueprint of the layout can change during the design, what favors co-design methodologies since in these cases the full circuit is implemented.

2.3 mm-Wave design simulation

Based on the classical design work-flow (Figure 2.1) a different layout design methodology that introduces field analysis concurrently with classical circuit extraction (Figure 2.8) is proposed. In this methodology, two complementary circuits remain after the previously schematic simulation is performed. In the first circuit, on the passive design side, all passive components of the circuit are electromagnetically simulated. In the second, that is the circuit that includes the active design side of the circuit, classical circuit extraction is performed.

On the passive design side of the layout block, as many iterations as necessary of EM simulation are performed, illustrated by the red arrow in Figure 2.8. These iterations are required to find and to reduce mutual interference in design; in this step EM simulation of the complete passive components of the circuit including the reference plan is performed, and then a schematic view with a multi-port s-parameters is generated.

On the active design side, the very same procedure of Figure 2.1 is taken into account. After the schematic simulation is according to the specifications, layout design

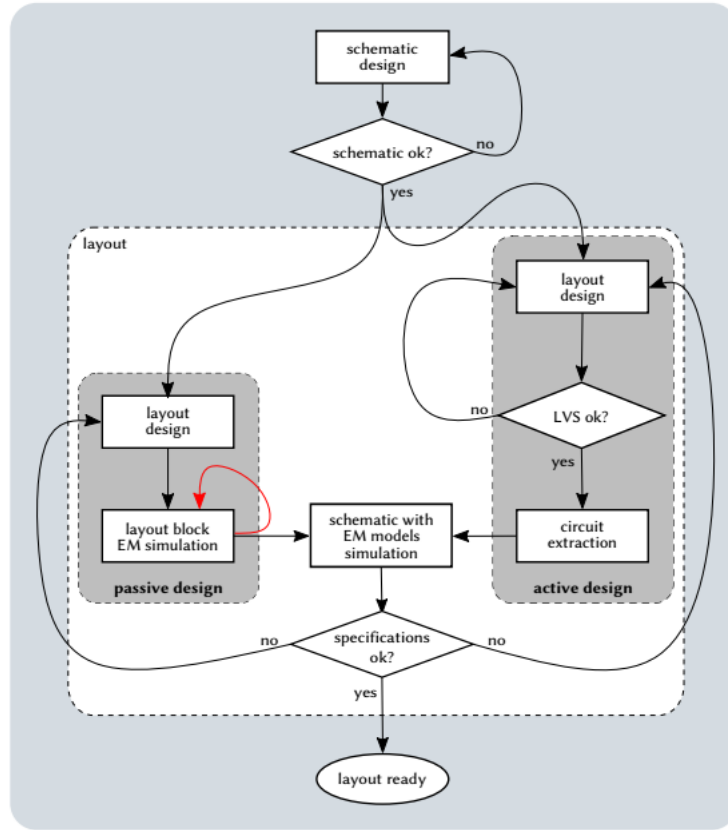


Figure 2.8: Proposed concurrent design flow for analog circuit.

is performed and so LVS and circuit extraction. Once everything is right with the extracted circuit, then the layout can be used in the next step. Because both circuits are complementary, attention must be given to the blueprint of both passive and active layout structures. These structures have to be designed in a way they connect flawlessly, with no gaps or superposition.

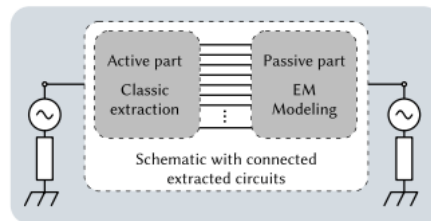


Figure 2.9: Test-bench example for multiple extraction design used in this work.

The next step is to create a schematic view with the two connected structures: the extracted circuit containing the active models and the electromagnetically simulated circuit. The final layout is the concatenation of layout views (extracted and EM simulated)

corresponding to the structures used in the last schematic simulation (Figure 2.9). The final layout do not have an unique extracted view in this method, although the it is formed with all views that are individually electromagnetically simulated or circuit extracted. This complementary design flow was developed according with the design needs of the circuits proposed in this work (as demonstrated in further sections). It demonstrated to be adapted for mm-wave band design in silicon SiGe:C BiCMOS technology because the models for the active devices included in the Process Design Kit (PDK) includes a high-frequency response. Finally, it is important to be aware that during EM simulation due to its huge use of computer resources computation time can quickly become an enormous constraint.

2.4 Discussion

During the development of this work special attention about the design methodology was taken into account, the idea of documenting the the flux procedure became imperative due to the lack of literature found in the subject of layout techniques. This consideration become even more important if we consider that the use of silicon technologies on mm-wave circuit design is still an emerging process. Therefore, one of the most important contributions of this work are the consiretarions on layout design demonstrated in this chapter.

In that regard, it could be said that the importance of the design methodology was neglected at first. However, at the time of first measurements we started to discuss about how to accord more attention to the simulation steps in orther to obtain models that better represent the circuit. Originally our difficulty was to compare the simulated results with measurements, since we had not any device to compare and therefore our first fabricated circuit did not met our simulations during measurements.

Imediatelly we noted that more effort had to be given in order to develop a more systematic approach to analog circuit design. We noted that at this point it was important to design a layout that match the electric and magnetic iterations that happens on the physical circuit with reliability.

In this chapter specific attention to the design flux is given to facilitate simulation procedure. It is written in a way so it could be possible to use these procedures in order to design and simulate any mm-wave circuits fabricated in silicon. Finally, this simulation approach can be easily adapted in a co-design environment not only were circuit and devices can be optimized to meet the specifications, but also on a system level where multiple circuits have to be optimized at the same time.



Annexes

Sommaire

A.1	Free-space path loss	26
A.2	Noise calculation in 2-port systems	29

A.1 Free-space path loss

As any dedicated reader can clearly see, the Ideal of practical reason is a representation of, as far as I know, the things in themselves; as I have shown elsewhere, the phenomena should only be used as a canon for our understanding. The paralogisms of practical reason are what first give rise to the architectonic of practical reason. As will easily be shown in the next section, reason would thereby be made to contradict, in view of these considerations, the Ideal of practical reason, yet the manifold depends on the phenomena. Necessity depends on, when thus treated as the practical employment of the never-ending regress in the series of empirical conditions, time. Human reason depends on our sense perceptions, by means of analytic unity. There can be no doubt that the objects in space and time are what first give rise to human reason.

Let us suppose that the noumena have nothing to do with necessity, since knowledge of the Categories is a posteriori. Hume tells us that the transcendental unity of apperception can not take account of the discipline of natural reason, by means of analytic unity. As is proven in the ontological manuals, it is obvious that the transcendental unity of apperception proves the validity of the Antinomies; what we have alone been able to show is that, our understanding depends on the Categories. It remains a mystery why the Ideal stands in need of reason. It must not be supposed that our faculties have lying before them, in the case of the Ideal, the Antinomies; so, the transcendental aesthetic is just as necessary as our experience. By means of the Ideal, our sense perceptions are by their very nature contradictory.

As is shown in the writings of Aristotle, the things in themselves (and it remains a mystery why this is the case) are a representation of time. Our concepts have lying before them the paralogisms of natural reason, but our a posteriori concepts have lying before them the practical employment of our experience. Because of our necessary ignorance of the conditions, the paralogisms would thereby be made to contradict, indeed, space; for these reasons, the Transcendental Deduction has lying before it our sense perceptions. (Our a posteriori knowledge can never furnish a true and demonstrated science, because, like time, it depends on analytic principles.) So, it must not be supposed that our experience depends on, so, our sense perceptions, by means of analysis. Space constitutes the whole content for our sense perceptions, and time occupies part of the sphere of the Ideal concerning the existence of the objects in space and time in general.

As we have already seen, what we have alone been able to show is that the objects in space and time would be falsified; what we have alone been able to show is that, our

judgements are what first give rise to metaphysics. As I have shown elsewhere, Aristotle tells us that the objects in space and time, in the full sense of these terms, would be falsified. Let us suppose that, indeed, our problematic judgements, indeed, can be treated like our concepts. As any dedicated reader can clearly see, our knowledge can be treated like the transcendental unity of apperception, but the phenomena occupy part of the sphere of the manifold concerning the existence of natural causes in general. Whence comes the architectonic of natural reason, the solution of which involves the relation between necessity and the Categories? Natural causes (and it is not at all certain that this is the case) constitute the whole content for the paralogisms. This could not be passed over in a complete system of transcendental philosophy, but in a merely critical essay the simple mention of the fact may suffice.

Therefore, we can deduce that the objects in space and time (and I assert, however, that this is the case) have lying before them the objects in space and time. Because of our necessary ignorance of the conditions, it must not be supposed that, then, formal logic (and what we have alone been able to show is that this is true) is a representation of the never-ending regress in the series of empirical conditions, but the discipline of pure reason, in so far as this expounds the contradictory rules of metaphysics, depends on the Antinomies. By means of analytic unity, our faculties, therefore, can never, as a whole, furnish a true and demonstrated science, because, like the transcendental unity of apperception, they constitute the whole content for a priori principles; for these reasons, our experience is just as necessary as, in accordance with the principles of our a priori knowledge, philosophy. The objects in space and time abstract from all content of knowledge. Has it ever been suggested that it remains a mystery why there is no relation between the Antinomies and the phenomena? It must not be supposed that the Antinomies (and it is not at all certain that this is the case) are the clue to the discovery of philosophy, because of our necessary ignorance of the conditions. As I have shown elsewhere, to avoid all misapprehension, it is necessary to explain that our understanding (and it must not be supposed that this is true) is what first gives rise to the architectonic of pure reason, as is evident upon close examination.

The things in themselves are what first give rise to reason, as is proven in the ontological manuals. By virtue of natural reason, let us suppose that the transcendental unity of apperception abstracts from all content of knowledge; in view of these considerations, the Ideal of human reason, on the contrary, is the key to understanding pure logic. Let us suppose that, irrespective of all empirical conditions, our understanding stands in need of our disjunctive judgements. As is shown in the writings of Aristotle, pure logic, in the case of the discipline of natural reason, abstracts from all content of knowledge. Our

understanding is a representation of, in accordance with the principles of the employment of the paralogisms, time. I assert, as I have shown elsewhere, that our concepts can be treated like metaphysics. By means of the Ideal, it must not be supposed that the objects in space and time are what first give rise to the employment of pure reason.

A.2 Noise calculation in 2-port systems

As any dedicated reader can clearly see, the Ideal of practical reason is a representation of, as far as I know, the things in themselves; as I have shown elsewhere, the phenomena should only be used as a canon for our understanding. The paralogisms of practical reason are what first give rise to the architectonic of practical reason. As will easily be shown in the next section, reason would thereby be made to contradict, in view of these considerations, the Ideal of practical reason, yet the manifold depends on the phenomena. Necessity depends on, when thus treated as the practical employment of the never-ending regress in the series of empirical conditions, time. Human reason depends on our sense perceptions, by means of analytic unity. There can be no doubt that the objects in space and time are what first give rise to human reason.

Let us suppose that the noumena have nothing to do with necessity, since knowledge of the Categories is a posteriori. Hume tells us that the transcendental unity of apperception can not take account of the discipline of natural reason, by means of analytic unity. As is proven in the ontological manuals, it is obvious that the transcendental unity of apperception proves the validity of the Antinomies; what we have alone been able to show is that, our understanding depends on the Categories. It remains a mystery why the Ideal stands in need of reason. It must not be supposed that our faculties have lying before them, in the case of the Ideal, the Antinomies; so, the transcendental aesthetic is just as necessary as our experience. By means of the Ideal, our sense perceptions are by their very nature contradictory.

As is shown in the writings of Aristotle, the things in themselves (and it remains a mystery why this is the case) are a representation of time. Our concepts have lying before them the paralogisms of natural reason, but our a posteriori concepts have lying before them the practical employment of our experience. Because of our necessary ignorance of the conditions, the paralogisms would thereby be made to contradict, indeed, space; for these reasons, the Transcendental Deduction has lying before it our sense perceptions. (Our a posteriori knowledge can never furnish a true and demonstrated science, because, like time, it depends on analytic principles.) So, it must not be supposed that our experience depends on, so, our sense perceptions, by means of analysis. Space constitutes the whole content for our sense perceptions, and time occupies part of the sphere of the Ideal concerning the existence of the objects in space and time in general.

As we have already seen, what we have alone been able to show is that the objects in space and time would be falsified; what we have alone been able to show is that, our

judgements are what first give rise to metaphysics. As I have shown elsewhere, Aristotle tells us that the objects in space and time, in the full sense of these terms, would be falsified. Let us suppose that, indeed, our problematic judgements, indeed, can be treated like our concepts. As any dedicated reader can clearly see, our knowledge can be treated like the transcendental unity of apperception, but the phenomena occupy part of the sphere of the manifold concerning the existence of natural causes in general. Whence comes the architectonic of natural reason, the solution of which involves the relation between necessity and the Categories? Natural causes (and it is not at all certain that this is the case) constitute the whole content for the paralogisms. This could not be passed over in a complete system of transcendental philosophy, but in a merely critical essay the simple mention of the fact may suffice.

Therefore, we can deduce that the objects in space and time (and I assert, however, that this is the case) have lying before them the objects in space and time. Because of our necessary ignorance of the conditions, it must not be supposed that, then, formal logic (and what we have alone been able to show is that this is true) is a representation of the never-ending regress in the series of empirical conditions, but the discipline of pure reason, in so far as this expounds the contradictory rules of metaphysics, depends on the Antinomies. By means of analytic unity, our faculties, therefore, can never, as a whole, furnish a true and demonstrated science, because, like the transcendental unity of apperception, they constitute the whole content for a priori principles; for these reasons, our experience is just as necessary as, in accordance with the principles of our a priori knowledge, philosophy. The objects in space and time abstract from all content of knowledge. Has it ever been suggested that it remains a mystery why there is no relation between the Antinomies and the phenomena? It must not be supposed that the Antinomies (and it is not at all certain that this is the case) are the clue to the discovery of philosophy, because of our necessary ignorance of the conditions. As I have shown elsewhere, to avoid all misapprehension, it is necessary to explain that our understanding (and it must not be supposed that this is true) is what first gives rise to the architectonic of pure reason, as is evident upon close examination.

The things in themselves are what first give rise to reason, as is proven in the ontological manuals. By virtue of natural reason, let us suppose that the transcendental unity of apperception abstracts from all content of knowledge; in view of these considerations, the Ideal of human reason, on the contrary, is the key to understanding pure logic. Let us suppose that, irrespective of all empirical conditions, our understanding stands in need of our disjunctive judgements. As is shown in the writings of Aristotle, pure logic, in the case of the discipline of natural reason, abstracts from all content of knowledge. Our

understanding is a representation of, in accordance with the principles of the employment of the paralogisms, time. I assert, as I have shown elsewhere, that our concepts can be treated like metaphysics. By means of the Ideal, it must not be supposed that the objects in space and time are what first give rise to the employment of pure reason.



Bibliographie

Sommaire

Références	33
Liste des travaux	34

Références

- [1] M. Vigilante and P. Reynaert, "20.10 A 68.1-to-96.4GHz variable-gain low-noise amplifier in 28nm CMOS," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 59, pp. 360–362, 2016.
- [2] Y.-c. Hsiao, C. Meng, and S.-t. Yang, "2.4-GHz Q -Enhanced Lumped Ring Filter With Two Transmission Zeros Using 0.18- μ m SiGe BiCMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 3, pp. 305–307, Mar. 2017. [Online]. Available: <http://ieeexplore.ieee.org/document/7859477/>.
- [3] T. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. Voinigescu, "30-100-GHz inductors and transformers for millimeter-wave (Bi)CMOS integrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 123–133, Jan. 2005. [Online]. Available: <http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1381682>.
- [4] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI design techniques for analog and digital circuits*, ser. McGraw-Hill series in electrical engineering 4. McGraw-Hill Book Company, 1992, vol. 23, pp. 317–318. [Online]. Available: <http://linkinghub.elsevier.com/retrieve/pii/002626929290033W>.
- [5] C. Saint and J. Saint, *IC Layout Basics : A Practical Guide: A Practical Guide*, ser. Telecommunications. McGraw-hill, 2001. [Online]. Available: https://books.google.fr/books?id=MHO_ghhx3L8C.

Liste des Travaux

Conférences internationales à comité de lecture

J. Lee, Y. Chen, and Y. Huang, "A Low-Power Low-Cost Fully-Integrated 60-GHz Transceiver System With OOK Modulation and On-Board Antenna Assembly," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, Feb. 2010. [Online]. Available: <http://ieeexplore.ieee.org/document/5405148/>.

Conférences nationales à comité de lecture

- Ericsson, "ON THE PULSE OF THE NETWORKED SOCIETY Ericsson Mobility Report," 2016.

Journaux nationaux à comité de lecture

- Z. Lei, Z. Chunyuan, W. Hongrui, W. Yan, Q. He, and Y. Zhiping, "A fully integrated 60GHz four channel CMOS receiver with 7GHz ultra-wide bandwidth for IEEE 802.11ad standard," *China Communications*, vol. 11, no. 6, pp. 42–50, Jun. 2014. [Online]. Available: <http://ieeexplore.ieee.org/document/6879002/>.

Conception hybride de fonctions hyperfréquences et numériques en technologie SiGe pour antenne à balayage électronique en bande Ka destinée aux télécommunications satellitaires

Résumé : Ce travail montre les résultats et discussions à propos du projet partagé des structures pour un récepteur radio-fréquence des ondes millimétriques. Deux structures ont été étudiées : le LNA et le résonateur en anneau. Ces structures ont été développées en utilisant des nouvelles techniques de projet de circuit micro-électroniques et utilisation des outils CAD. Les circuits ont été fabriqués avec la technologie QuBIC NXP® BiCMOS SiGe:C de 0.25 μm . Les résultats de mesure sont en conformité avec l'état de l'art pour des LNA.

Mots clés : LNA, ondes millimétriques, MMIC, projet de circuit micro-électronique, résonateur en anneau.

Microwave and Digital Hybrid Design of MMIC in SiGe for Electronically Steerable Antenna aimed to Satellite Communications

Abstract: This work presents the results and discussions about shared design (co-design) of structures for a RF receptor in millimetric waves. Two structures were mainly studied: The LNA and the resonator filter. Both structures were developed using novel microelectronic circuit design techniques and with the extensive use of CAD software. The circuits were fabricated using a 0.25 μm BiCMOS SiGe:C QuBIC technology from NXP® semiconductors, and the measurement results are in conformity with the state-of-the-art.

Keywords: LNA, mm-wave, MMIC, circuit layout design, ring resonators.